PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-141633
(43)Date of publication of application : 17.05.2002

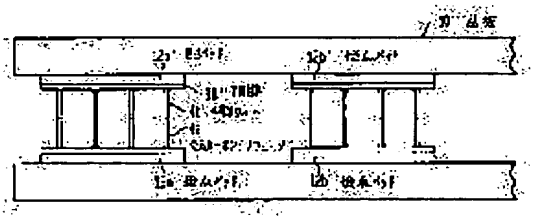
(51)Int.Cl. H05K 1/14
B82B 1/00
B82B 3/00
H01L 23/52
H05K 3/36
// C01B 31/02
C23C 16/26

(21)Application number : 2000-324945
(22)Date of filing : 25.10.2000

(71)Applicant : LUCENT TECHNOL INC
(72)Inventor : BROWN WALTER L
JIN SUNGHO
ZHU WEI

(54) ARTICLE COMPRISING VERTICALLY NANO-INTERCONNECTED CIRCUIT DEVICE AND METHOD FOR MAKING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an equi-length nanowire and a circuit device vertically interconnected by the nanowire.
SOLUTION: This vertically interconnected circuit device is provided. The circuit device has at least two circuit layers, and a plurality of equi-length nanowires arranged between the circuit layers. The nanowires comprise composites having a heterojunction present along the length thereof to provide for a variety of device applications. This method for making the circuit device includes a step for growing the plurality of nanowires on a removable substrate (a), a step for equalizing the length of the nanowires and for making the length of each of the plurality of nanowires nearly equal (b), a step for transferring and joining exposed ends of the plurality of nanowires to a first circuit layer (c), and a step for removing the substrate (d). The nanowire joined to the first circuit layer is further joined to a second one, thus forming the vertically interconnected circuit device.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The product characterized by having the circuit device which is arranged between two circuitry layers even if there are not at least two circuitry layers and these **, and interconnects two circuitry layers electrically even if this ** cannot be found, and which consists of a nano wire of two or more in general equal die length.
[Claim 2] The product according to claim 1 characterized by what each diameter of two or more of said nano wires is less than 500nm.
[Claim 3] The product according to claim 1 characterized by what each of two or more of said nano wires has aligned in general perpendicularly.
[Claim 4] With at least two circuitry layers, it is arranged perpendicularly, and has the circuit device which consists two circuitry layers of a nano wire of two or more in general parallel and equal die length which interconnects electrically even if this ** cannot be found. It is the product characterized by for each diameter of two or more of said nano wires being less than 500nm, and each of two or more of said nano wires being joined to one side of said at least two circuitry layers by the metal soldered joint.
[Claim 5] Said two or more nano wires are products according to claim 4 characterized by what mechanical comp rye ANSI for avoiding the integrity problems relevant to external force is shown for.
[Claim 6] Said two or more nano wires are products according to claim 4 characterized by what is chosen from the group which consists of a nano wire formed from a carbon nanotube, a semi-conductor nanotube and metals, alloys, oxides, nitrides, borides, or at least one kind in the mixed ceramics.
[Claim 7] The product according to claim 4 with which the one die length of the arbitration of said nano wires is characterized by what is deviated from all the average die length of two or more of said nano wires to less than 20%.
[Claim 8] At least one in said two or more nano wires is the product according to claim 4 characterized by what is consisted of a compound nano wire which has the heterojunction which exists along with the die length.
[Claim 9] (a) Each of the step which prepares a substrate, and the nano wire of (b) plurality so that it may have the 1st exposure edge and the 2nd edge combined with said substrate So that each die length of the step which grows up two or more nano wires on said substrate, and the nano wire of the (c) aforementioned plurality may become in general equal The step which makes the die length of said nano wire isometry-ize, and the step which joins said 1st exposure edge of the nano wire of the (d) aforementioned plurality to the 1st circuitry layer, (e) The manufacture approach of the circuit device characterized by what is consisted of a step which removes said substrate in order to form the circuit device which has said two or more nano wires joined to said 1st circuitry layer, with the 2nd edge of two or more of said nano wires exposed.
[Claim 10] Said substrate removal step is an approach according to claim 9 characterized by what is consisted of separating mechanically the 2nd edge of two or more of said nano wires from said substrate.
[Claim 11] It is the approach according to claim 9 which said substrate consists of a soluble substrate and is characterized by what said substrate removal step consists of dissolving said substrate chemically.
[Claim 12] (f) The approach according to claim 9 characterized by what it has further for the step which prepares the 2nd circuitry layer, and the step which makes said 2nd circuitry layer join said 2nd exposure edge to the step which covers the 2nd exposure edge of two or more of said nano wires with the 2nd solder ingredient in order to form the circuit device which interconnected in (g) (h) perpendicular.
[Claim 13] The growth step of two or more of said nano wires is an approach according to claim 9 characterized by what a catalyst nucleation layer is made to put on said soluble substrate, and is consisted of decomposing the gas which adjoined said catalyst nucleation layer.

[Claim 14] Said gas is an approach according to claim 13 characterized by what is consisted of hydrocarbon content gas so that a carbon nanotube may grow on said soluble substrate.
[Claim 15] (i) Approach according to claim 9 characterized by what it has further for the step which covers a solder ingredient at either [at least] the 1st of two or more of said nano wires, or the 2nd exposure edge.
[Claim 16] The approach according to claim 15 characterized by what said soluble substrate is rotated for in order to apply said solder ingredient to either [at least] the 1st of two or more of said nano wires, or the 2nd exposure edge by vacuum evaporationo and to promote homogeneity spreading on said two or more nano wires of said solder ingredient in that case.
[Claim 17] Said 1st and 2nd circuitry layers are approaches according to claim 15 characterized by what it has two or more contact pads, a solder ingredient layer is respectively applied to each contact pad on said 1st and 2nd circuitry layers, and the 1st and 2nd edges of two or more of said nano wires are joined for to said contact pad.
[Claim 18] The 1st solder ingredient used in order to join said 1st exposure edge to said 1st circuitry layer has the 1st soldering temperature. The 2nd solder ingredient used in order to join said 2nd exposure edge to said 2nd circuitry layer is an approach according to claim 17 which has the 2nd soldering temperature and is characterized by the thing with said 2nd soldering temperature lower than said 1st soldering temperature.
[Claim 19] The step which makes the die length of said nano wire isometry-ize (i) The step which said two or more nano wires combined with said soluble substrate are partially embedded [step] into the sacrifice ingredient layer of in general uniform thickness, and makes the excessive die-length part of a nano wire project from said sacrifice ingredient by that cause, (ii) Approach according to claim 9 characterized by what is consisted of a step which removes the excessive die-length part of said nano wire, and a step which removes said (iii) sacrifice ingredient.
[Claim 20] The approach according to claim 19 characterized by what it has further for the conductive substrate layer put in between between said soluble substrate used in order to heighten the adhesive strength to said soluble substrate of said sacrifice ingredient layer, and said catalyst nucleation layer.
[Claim 21] Said sacrifice ingredient is an approach according to claim 19 characterized by what is put by electroplating.
[Claim 22] The thickness of said sacrifice ingredient layer is an approach according to claim 19 characterized by what is been within the limits of about 1-100 micrometers.
[Claim 23] The average diameter of two or more of said nano wires is a product according to claim 1 which is less than 200nm and is characterized by what either [at least] semi-conductor p-n junction or the tunnel junctions are contained for.
[Claim 24] The product which consists of an array of the nano wire rectifier-diode device by claim 1 which interconnected perpendicularly.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the structure which nano interconnect was carried out or manufactures the circuit by which the nano package was carried out, and its manufacture approach. Furthermore, this invention relates to the perpendicular electrical connection which used the conductive nano wire at a detail.
[0002]
[Description of the Prior Art] A nano-scale wire like the carbon nanotube which has the very minute size scale whose diameter is 1-100 nanometers, and whose die length is about 0.1-100 micrometers is capturing the big spotlight recently. Such a nano-scale wire for example Liu etal. and SCIENCE, Vol.280 and p.1253; (1998) Ren et al. and SCIENCE, Vol.282 and p.1105; (1998) Lie et al. and SCIENCE, Vol.274 and p.1701; (1996) Frank etal. and SCIENCE, Vol.280 and p.1744; (1998) J.Tans et al. and NATURE, Vol.36 and p.474; (1997) Fan et al. and SCIENCE, Vol.283 and p.512; (1999) Collins etal. and SCIENCE, Vol.278 and p.100; (1997) It is indicated by Kong et al., NATURE, Vol.395, p.878; (1998) and Ebbensen et al., NATURE, Vol.382, p.54, etc. (1996).
[0003] A carbon nanotube shows peculiar atomic arrangement, nano-scale structure, and interesting physical properties (for example, single dimension electric behavior, quantum conductance, impact transport properties, etc.). or [that the impact transportation in a carbon nanotube is equal to the current density in some superconductors as reported by Frank and others] -- or it is the current density of the magnitude to exceed and a huge current is enabled to pass through the inside of an electronic circuitry. A carbon nanotube is an example of the nano wire ingredient of the lower limit, generally, a high aspect ratio and in the case of a single wall nanotube, has a -1nm small diameter, and, in the case of a multiwalled nanotube, has a diameter below -50nm. These are indicated by Rinzler et al, APPLIED PHYSICS, Vol.A67, p.6612 and (1994) Kiang et al, PHYSICAL REVIEW LETTERS, Vol.81, and p.1869 (1998).
[0004] Generally the single wall carbon nanotube of high quality grows in the random direction with laser ablation or an arc technique as needlelike or a nanotube whose shape of spaghetti tangled. (In order to remove non-nanotube matter, such as a graphite or amorphous phase, and catalyst metal, generally about the generated carbon nanotube by the arc technique, chemical purification processing is required.) chemical vapor growth (CVD) which was used by Ren et al., Fan et al., Li and others -- law tends to generate the multiwalled nanotube adhering to a substrate In this case, perpendicular half-alignment or the parallel growth which aligned is often shown to a substrate. A carbon nanotube will be generated by catalyst disassembly of hydrocarbon content precursors, such as ethylene, methane, or benzene, if reaction parameters, such as temperature, time amount, precursor concentration, and a flow rate, are optimized as indicated by these reference. A nucleation layer like the tin coat of nickel, Co, and Fe is added to a substrate front face often intentionally, and carries out nucleation of various isolation nanotubes. Moreover, a carbon nanotube can also be made carry out nucleation and grown up on a substrate by using the hydrocarbon content precursor mixed with the chemical entity (for example, ferrocene) containing one or more kinds of these catalyst metal atoms, without using the above metal nucleation layers. In chemical vapor growth, these metal atoms promote the nucleation of the nanotube to a substrate side. This is indicated by Cheng et al., CHEM.PHYSICS LETTERS, Vol.289, and p.602 (1998).
[0005] The latest inclination in an electronic circuit design, interconnect, and packaging is going in the direction which uses a much more detailed feature (feature). Such submicron feature size is the size which recently reached just. In order to generate desired super-high density electronic packaging, circuit Rhine of minute line breadth is important like the three-dimension multilayer configuration of having the circuitry

layer accumulated perpendicularly. However, the nano wire which grew by the approach available now is unsuitable for such the purpose. A single wall nanotube (SWNT) so that it may generally be compounded [grown-up] by laser ablation or the arc technique has a spaghetti-like configuration, tangles often mutually and suits. A multiwalled nanotube (MWNT) which was generally formed of chemical vapor deposition can be generated still more easily in the parallel configuration which aligned. However, nanotubes so that it may be reported [these / grown-up] by Ren et al., Li and others differ in height or die length. In circuit interconnect of high-reliability without an electric short circuit or disconnection, it is desirable to generate the nanotube which has equal predetermined die length. Furthermore, it is convenient to form a nanotube as a self-standing wire. Consequently, these nanotubes can be elaborately operated about migration, arrangement, bonding, etc. for the circuit interconnect in a room temperature or comparatively low temperature (for example, 300 degrees C or less). Alternative CVD growth of a nanotube like the carbon nanotube which grew directly on the desired circuit pad can be carried out using alternative area patterning of a catalyst bed. However, when the most, it is not desirable to expose a delicate semiconductor circuit and a delicate component to an elevated temperature (for example, 600-1000 degrees C) and the chemistry environment accompanying a CVD deposit of a nanotube.

[0006]

[Problem(s) to be Solved by the Invention] Therefore, the purpose of this invention is offering the circuit device which interconnected perpendicularly using the nano wire and such a nano wire of in general equal die length which can be formed as a suitable self-standing unit for convenient perpendicular interconnect.

[0007]

[Means for Solving the Problem] Said technical problem is solved by the circuit device which has at least two circuitry layers and the nano wire of two or more in general equal die length arranged between these circuitry layers and which interconnected perpendicularly. The nano wire of this invention consists of a composite which has the heterojunction which exists along with the die length, for example, and can be used for many device applications. Moreover, the step grown up on the substrate from which the manufacture approach of the circuit device of this invention can remove the nano wire of (a) plurality, (b) (c) migration is carried out with the step made to equate the die length of a nano wire (for example, each die length of two or more nano wires becomes in general equal as a result), and it consists of the step which joins the exposure edge of two or more nano wires to the 1st circuitry layer and the step which removes the (d) substrate. The circuit device which interconnected in the perpendicular can be formed by joining further the nano wire joined to the 1st circuitry layer to the 2nd circuitry layer.

[0008]

[Embodiment of the Invention] This invention relates to the manufacture approach of a conductive nano wire like a carbon nanotube. This carbon nanotube is useful as a connection wire within the flat surface between adjoining electric contact pads as a wire for perpendicular junction of a nano-scale between circuit device layers. In circuit interconnect like a fitting device between [of two] circuitry layers, use of the parallel electric conduction pass with which a large number were subdivided is attained by the nano wire which aligned. a nano wire -- for example, ** -- since better, it provides with the elastic compliance and flexibility of a convenient interconnect medium avoiding integrity problems the short-term dependability generated with colander stress, and over a long period of time. The source of common stress continuously added to an interconnect medium over a long period of time is machine stress, thermal stress, etc. which are introduced during for example, a partial temperature gradient, the stress which occurs by the mismatch of the coefficient of thermal expansion between different ingredients currently used within the device, electronic migration valence stress and the assembly of a device, handling, a trial, or transportation. or [avoiding the integrity problems which occur with stress, such as fatigue of an interconnect medium or passive circuit elements, a creep, or deformation breakage, according to this invention] -- or it can minimize. When using the nano wire of a minute diameter, this invention is useful although high density or super-high density circuit interconnect is attained.

[0009] Drawing 1 A - 1D is the mimetic diagram of the nano wire of various configurations which grew on the substrate 10. A nano wire can consist of nano wires formed in these contractors, such as the semi-conductor nano wire formed of a carbon nanotube, for example, Si and germanium, or GaAs or metals, alloys, oxide, carbide, nitrides, borides, or mixed ceramics, from the conductivity of well-known others, or a non-conductive ingredient. The manufacture approach of a nano wire consists of chemical vapor growth of laser ablation, arc discharge, precursor gas, or a precursor gas mixture object etc. Nucleation of the minute diameter nano wire can be carried out by catalyst decomposition of a gaseous phase, and it can be grown up upwards from a substrate. In this case, a catalyst thin film is vapor-deposited on a substrate, and it is made to

start by understanding the partial nucleation of this thin film by the catalyst in a gaseous phase. For example, the glass circuit board can be prepared, the catalyst thin film which consists of transition metals can be vapor-deposited on a glass substrate, and, subsequently a carbon nanotube can be formed by decomposing C2H4 on this thin film substrate. This catalyst thin film is also called a catalyst nucleation thin film in this specification, and can constitute this thin film from an ingredient of well-known others to nickel, Co, Fe, or this contractor.

[0010] As shown in drawing 1 A and drawing 1 B, respectively, it grows up toward a random direction, or when there is no alignment processing, a nano wire tends to grow so that it may tangle each other (tangle). The gestalt (drawing 1 B) whose nano wire 14' tangled is acquired also by use of laser ablation. However, in order to use it with sufficient convenience in perpendicular interconnect, as for a nano wire, having aligned in general perpendicularly is desirable. For example, by use of impression electric field, gas concentration inclination, or a temperature gradient, a nano wire can respond for forming and a nano wire can be aligned. moreover, the physical technique which uses the cavity perpendicular cavity in a substrate -- or it can respond for making it grow up by high density-ization (for example, coincidence formation of the "jungle" (for example, high concentration per unit area) of a nano wire), and a nano wire can be aligned. In order to promote alignment growth of a nano wire, a porosity ceramic or a silicon layer can also be used together with a catalyst nucleation thin film. As shown in drawing 1 C, an alignment nano wire can be uneven die-length 14", or as shown in drawing 1 D, it can be the uniform die length 14. A mode, i.e., a nano wire, as shown in drawing 1 D aligns in general, and a mode which is in general equal die length is desirable. As for the die length of each nano wire, it is desirable to change only to less than 10% much more preferably from average nano wire die length to less than 20%.

[0011] As for the nano wire 14, it is desirable to align perpendicularly to a substrate and to be arranged in general by juxtaposition. Completely perpendicular alignment (for example, the include angle phi between the front face 11 of a substrate and the die length of a nano wire should be 90 degrees to be shown in drawing 1 D) of a nano wire is unnecessary. However, the minute thing of the fluctuation from perfect perpendicular alignment is desirable. That is, less than about 25 degrees of this fluctuation are less than 15 degrees preferably from perfect perpendicular (90 degrees) alignment.

[0012] In order to easy-ize use in formation of perpendicular interconnect, it can be made to grow up on another substrate which can dissolve a nano wire. For example, drawing 2 shows perpendicular alignment nano wire 14" of the uneven die length on the soluble substrate 22 which grew using the catalyst nucleation thin film 26. A soluble substrate helps a move of the nano wire in formation of circuit interconnect so that it may explain below. A soluble substrate layer can be dissolved in water, an acid, a base, or a solvent. For example, a sodium chloride crystal can be used and a water-soluble substrate can be formed. In order to form an acid solubility substrate, metals, such as Cu, nickel, Co, Mo, Fe, V, Au, Ag, or these alloys, can be used. In order to form a base solubility substrate, the metals like aluminum can be used. For example, a substrate must be chosen so that the nano wire growth temperature by the CVD method may become below the melting point of the substrate ingredient used. In order to form another substrate layer as an exception method, a soluble polymer ingredient can also be used. Such a polymer ingredient is polyvinyl alcohol, polyvinyl acetate, polyacrylamide, acrylonitrile styrene butadiene rubber, or volatile matter (for example, polymethylmethacrylate (PMMA)). When using a polymer, the temperature used in processing of a nano wire must be temperature low enough, in order to avoid damage on polymers, such as decomposition, change of a physical configuration, or change of a chemistry property. A soluble substrate layer can also be formed also by using an ingredient together. In order to grow up a nano wire, the catalyst nucleation thin film 26 (for example, nickel, Fe, or Co) can also be covered to a soluble substrate. A soluble substrate is removable after a nano wire grows. A catalyst nucleation thin film can be made to deposit on a soluble layer with the spot pattern-gestalt as a continuation layer by sputtering, vacuum evaporationo, or electrochemistry plating.

[0013] As shown in drawing 1 C and drawing 2 , a nano wire can form the nano wire of in general equal die length by making it grow up to be uneven die length at first, and subsequently performing isometry-ized processing, as shown in drawing 1 D. As mentioned above, the nano wire of equal die length is desirable. This is indicated by for example, the United States patent application/[09th] No. 354928 specification. An example of the isometry-ized approach is typically illustrated by drawing 3 A - drawing 3 D. The merit-ized approaches -- it can set in this example -- consist of three steps in general. (1) -- it consists of the step (drawing 3 A-3B) which embeds the nano wire of uneven die length in the soluble sacrifice layer 30 of in general uniform thickness, a step (drawing 3 C) which removes the excessive die length 34 of the nano wire which has projected from (2) sacrifice layers, and a step (drawing 3 D) which removes (3) sacrifice layers.

[namely,] Needless to say, the isometry-ized approach of others, such as laser beam cutting and hot blade cutting, can also be used. This is indicated by the United States patent application/[09th] No. 236933 specification.

[0014] By the approach in the example of drawing 3 A - 3D, the 1st step is making the sacrifice layer of in general uniform thickness deposit. Drawing 3 A shows how to make the sacrifice layer 30 deposit on the substrate 22 which has nano wire 14" of electroplating equipment and uneven die length. The copper (Cu) solubility substrate layer 22 is prepared, and the catalyst nucleation thin film 26 which consists of nickel (nickel) whose thickness is about 1-100nm is made to deposit on this substrate layer in this example. Needless to say, the ingredient of above others can also be used for the soluble substrate layer 22 or the nucleation thin film 26. In drawing 3 A, the catalyst nucleation thin film 26 is illustrated as a continuation layer. However, a catalyst nucleation thin film may be fractured by the shape of a fragment, and island shape when heated in chemical vapor growth and nano wire growth (even if it is the case where it has deposited as for example, a continuation layer). Such fragmentation of a catalyst nucleation thin film leaves the front face of a soluble substrate between the nano wires which decreased in number, without putting a conductive metal membrane. According to the ingredient which constitutes a soluble substrate, it is sometimes difficult to cover the metal sacrifice layer 30 to a substrate and a fragmentation catalyst nucleation thin film (drawing 3 C and the following explain). This is the case [like] where for example, a soluble substrate is insulation (for example, it consists of sodium chlorides). Therefore, before making a catalyst nucleation thin film deposit, a non-catalyst nature conductivity substrate layer (not shown) can be made to deposit first on a soluble substrate. If it puts in another way, a substrate layer can be made to put in between between the soluble substrate 22 and the catalyst nucleation thin film 26 in drawing 2 . This substrate layer can consist of non-catalyst nature conductivity ingredients of well-known others to Mo or this contractor.

[0015] Cu substrate layer 22 functions as a cathode in this approach, adjoins an anode 24 (for example, nickel anode), and is arranged in the electrolyte bath 25 combined with the anode by the power source 23. The electrolyte 25 contains the ion of the metal which should be deposited. For example, nickel is made to deposit from a NiSO4 content solution, or Cu is made to deposit from CuSO4 solution. As for the electrolyte bath 25, it is desirable to contain the ion of the catalyst nucleation thin film 26 or a conductive substrate layer and ion same type. thus, a chemical affinity -- electroplating of the sacrifice layer 36 -- nano wire 14" (for example, carbon or a silicon nano wire) -- it is not upwards and happens on the front face of the catalyst nucleation thin film 26. For example, the sacrifice layer 30 has the same metal property as a catalyst nucleation thin film, and a nano wire has a sharply different property. A sacrifice layer is deposited even on the in general same thickness as the die length of a request of a nano wire. Although this parameter (nano wire die length) changes according to application of a desired sensor, generally it is within the limits of 1-100nm as mentioned above. The thickness of a sacrifice layer is controllable by activity variables, such as time amount, electrolytic concentration, and current density. Needless to say, drawing 3 A only shows an example of the approach of depositing a sacrifice layer. A sacrifice layer can be made to deposit also by the approach of others like electroless deposition, chemical vapor growth, or a physical vapor deposition (for example, sputtering, vacuum evaporationo, laser ablation, or ion beam vacuum evaporationo).

[0016] Drawing 3 B is the sectional view of the structure obtained by the electroplating approach of drawing 3 A. this -- the structure -- solubility -- a substrate -- a layer -- 22 -- a catalyst -- nucleation -- a thin film -- 26 -- in general -- being uniform -- thickness -- a sacrifice -- a layer -- 30 -- inside -- embedding -- having had -- being uneven -- die length -- nano -- a wire -- 14 -- " -- from -- becoming . Each nano wire 14" has the exposed excessive die-length part 34 which projects exceeding the sacrifice layer 30. In case the excessive die-length part 34 is removed, the sacrifice layer 30 protects a flasking nano wire temporarily. As for a sacrifice layer, it is desirable to consist of removable ingredients easily. Such an ingredient is an ingredient which can be removed by making it evaporate with the ingredient or heating which can be removed by the ingredient, chemical etching, or electrochemistry etching which can be removed by dissolving for example, a sacrifice layer in water or a solvent. Suitable water solubility or a solvent fusibility ingredient is salts like a sodium chloride, a silver chloride, a potassium nitrate, a copper sulfate, and indium chloride or sugar, and the organic substance like a glucose. The suitable ingredients which can be etched are the metals like Cu, nickel, Fe, Co, Mo, V, aluminum, Zn, In, Ag, Cu-nickel, and nickel-Fe, and alloys chemically. Dissolution removal of the sacrifice layer formed from these ingredients can be carried out with a basic solution like a hydrochloric acid, an aqua regia, an acid like a nitric acid, a sodium hydroxide, or ammonia. A suitable vaporizable ingredient is an ingredient which can be made to disassemble or incinerate by heat-treating in suitable oxidation like the ingredient in which high vapor pressure like Zn is shown, or organic acids,

reduction, or a natural gas ambient atmosphere.
[0017] As shown in drawing 3 C, the next step of the isometry-ized approach removes the exposed part 34 of a nano wire, and consists of obtaining the long nano wire 14, such as having been embedded in the sacrifice layer 30. This removal can be carried out chemical or by grinding or etching the exposed part 34 by the mechanical approach, for example. When the carbon nano wire is used, heat-treatment can also be used for removal of an exposed part, and this heating is a desirable art. For example, the excessive die-length part 34 is removable by being the temperature within the limits of 200 degrees C - 1000 degrees C, and heating this structure in an oxidizing atmosphere. perfect **** -- partial oxygen or an ozone ambient atmosphere can be used. In order to remove the excessive die-length part of a nano wire as an exception method, a mechanical polish approach can also be used. sacrifice layer 30' (refer to drawing 3 C) which has an isometric nano wire in the following step -- for example, it removes by making it dissolve. Thus, the substrate 22 as shown in drawing 3 D, and the structure which has the nano wire 14 of die length in general equal to the catalyst nucleation thin film 26 are obtained.
[0018] In case sacrifice layer 30' is removed, the catalyst nucleation thin film 26 must remain on the soluble substrate 22. It is because a nano wire will dissociate from a substrate 2 if the catalyst nucleation thin film 26 does not remain. When a sacrifice layer consists of a nonmetal layer like a sodium chloride, a copper sulfate, or polyvinyl alcohol, a sacrifice layer can be removed where a catalyst nucleation thin film is left, while it has been unhurt. However, when a sacrifice layer consists of a metal layer, a catalyst nucleation thin film will also remove removal of a sacrifice layer so that according to acid etching, consequently a nano wire will be separated from a substrate. in order to deal with this problem -- a sacrifice layer -- being partial (for example, the one half or 1/3 of the original thickness) -- it etches and the nano wire of sufficient die length to connect the exposed part of a nano wire to a circuit device is exposed. When removing a soluble substrate and a catalyst nucleation thin film in this case, the remaining sacrifice layers can be removed ex post. In order to protect a soluble substrate from deformation, the dissolution, etc., it is [in / an intermediate-processing-intermediate-treatment step] desirable to cover this soluble substrate with a temporary protective layer (not shown). This temporary protective layer can be applied to the tooth back and/or side face of a soluble substrate. Although this temporary protective layer is easily removed by the solvent (for example, alcohol or an acetone), it becomes a water solution from an ingredient stable lacquer type. The ingredient which constitutes the fusibility substrate 22, the catalyst nucleation thin film 26, and the sacrifice layer 30 is chosen so that it may have a fully different etch rate or a fully different removal rate. It is avoidable that this avoids that a catalyst nucleation thin film is dissolved by removal of a sacrifice layer, and/or a soluble substrate is damaged during processing.
[0019] For example, a long juxtaposition nano wire, such as having been held by the soluble substrate as shown in drawing 3 D, is useful for various device applications, such as perpendicular nano-scale circuit interconnect and a TAKUCHIKKU sensor device. About a certain application, it is conductivity electrically and the thin film or coat 36 (refer to drawing 4 A - 4C) of a joinable metal (soldering is possible) or an alloy can be preferably applied to some nano wires [at least]. By the case, an adhesion promotion layer (not shown) can also be arranged between a coat 36 and the nano wire 14. Metallizing processing of a nano wire is useful although conductivity is secured along the die-length direction of a nano wire. Some nano wires [at least] can be plastered with a coat 36. A coat 36 consists of a thin film of the metal (it can solder) which is conductivity, and it can be desirable and can be joined, or an alloy. A coat 36 is a solder alloy thin film like the metal thin film or Au-Sn in which soldering like Au, Ag, Pd, Rh, nickel, Cu, In, or Sn is possible, Sn-Ag, Pb-Sn, Bi-Sn, In-Sn, or In-Ag. In the case of a carbon nanotube or a nitride type nano wire, the adhesion promotion middle class between a coat and a nano wire can consist of carbide or a nitride generation element (for example, Ti, Mo, Nb, V, Fe, W, Zr). The layer which can be soldered, and an adhesion promotion layer can be made to add to a nano wire front face by many arts. Such an art is the combination of physical vapor deposition (sputtering, vacuum evaporationo, ion beam vacuum evaporationo), chemical vapor deposition, non-electrolyzed electrodeposition, electroplating, or the deposition approach etc. As an exception method, can be ****(ed) in solder or the coat layer itself which can be soldered, and an adhesion promotion element can also be made to **** in advance as an alloy element. In order to heighten further the adhesive strength between a nano wire front face and a deposition adhesion promotion layer or between an adhesion promotion layer and the layer which can be soldered, the optional improvement heat-treatment in adhesive strength can also be added. Such heat-treatment consists of heating at about 100-900 degrees C in inactive or a vacuum ambient atmosphere for 0.1 to 100 hours.
[0020] Drawing 4 A - 4C is the outline sectional view showing the metal coat 36 applied by various approaches. For example, drawing 4 A shows the condition of carrying out the line-of-aim vacuum

evaporationo of the metal atom with physical vapor deposition. This vacuum evaporationo is performed along a longitudinal direction according to an arrow "d" so that a metal may focus on one nano wire side. In order to make homogeneity vapor-deposit further over the whole front face of a nano wire, it can obtain by the strange method by rotating a substrate during vacuum evaporationo. The electrochemistry approach (for example, electrolytic plating or electroless deposition) of making a metal depositing can form the deposit localized alternatively, as shown in drawing 4 B. This alternative deposition can be made to occur with the high electrolytic concentration near the tip of a nano wire generally. An ununiformity profile is also obtained by the CVD approach. The homogeneity of a coat changes according to various processing parameters. Such a parameter is a rate which migration to the deposition part of a rate and a gas atom where a metal ion moves, and a coat deposit. By the deposition controlled much more careful slowly, as shown in drawing 4 C, along with the die length of a nano wire, the in general uniform metal coat 36 can be obtained. Generally, the thickness of a request of a metal layer or the layer which can be soldered, and a middle adhesion promotion layer (accepting the need) is within the limits of 0.5-50nm, and it is desirable that it is within the limits of 1-20nm.

[0021] The metal coat covered by the nano wire achieves some important functions.

(1) A metal coat gives the soldering possibility for joining a nano wire to the circuit board. The metal which can be soldered, or a solder alloy coat is desirably added also to the front face of the electric contact pad which should be joined to a nano wire.

(2) A metal coat gives uniform conductivity especially to a nonmetal nano wire, for example, a semi-conductor carbon nanotube, a semi-conductor nano wire (for example, Si or Ga-As), an insulating nano wire (for example, aluminum 2O3, SiO2, BN), or other insulating ceramic nano wires. It is efficient, and when forming highly reliable perpendicular interconnect, the stable electrical continuity from the end of the nano wire combined with a lower circuit device through the die length of a nano wire to the other end of the nano wire joined to an up device or an up circuitry layer is important. or [that a single wall nanotube is metallicity which has the "armchair" configuration of a carbon atom] -- or "zigzag" -- they can be the semi-conductor of the configuration of a type, or an of a certain kind "chiral" configuration - abbreviation insulation. Dresselhous et al., Science of Fullerines and Carbon Nanotubes, Chap.19 (Academic Press and San Diego 1996), pp.758, 805 -809 reference. Changing nanotube atomic arrangement and an electrical property dramatically along with the die length of a single carbon nanotube is known. Collins et al., SCIENCE, Vol.278, and p.100 Reference (Oct.3, 1997). Fluctuation of such an electrical property has a bad influence on the efficient electronic transportation between the nano interconnect devices through a carbon nanotube interconnect medium. The metal surface lining on the above nano wires solves this trouble, and gives desired conductivity to a perpendicular nano interconnect medium.

(3) When exposed to an environment or a processing ambient atmosphere, this metal coat also gives corrosion resistance/oxidation resistance to the coat which can be soldered, and when a nano wire tends to receive corrosion/oxidation, it gives corrosion resistance/oxidation resistance also to the nano wire itself further. Noble-metals thin films, such as Au, Ag, Pd, and Rh, can be used also as additional finishing to the top face of the metal coat 36 which could use it also as the coat itself or was put on the nano wire and which can be soldered. During soldering processing, thin finishing of noble metals like Au can be made to absorb easily in lower melting solder (for example, Au-Sn or Pb-Sn eutectic-mixture solder), consequently does not block junction.

[0022] Drawing 5 A - 5E is a mimetic diagram which illustrates an example of the approach of making join a nano wire to a substrate and forming perpendicular interconnect. As shown in drawing 5 A, the soluble substrate 22 which has the nano wire 14 of the in general equal die length with which the metal coat which can be soldered was covered is arranged to an upside-down. It arranges so that the circuit board 10 which has the contact pads 12a and 12b may be made to meet a nano wire. The ingredient used for formation of a contact pad can be chosen from the conductive ingredients which are generally used by semiconductor circuit manufacture like aluminum, Cu, W, Ta, TiN, TaN, and CoSi2 and from which a large number differ. An additional surface conductive film can also be used by the case. Moreover, it is desirable to cover the layer 38 which can be soldered to a contact pad. Generally, the area of the contact pads 12a and 12b etc. is less than [25 micrometers] two, is less than [1 micrometer] two preferably, and is less than [0.01 micrometers] two much more preferably.

[0023] In drawing 5 B, it changes a nano wire into the condition of having contacted the contact pad physically, and it heats the front face, and joins a nano wire with solder to a contact pad. In order to avoid crushing of the nano wire by the weight of a substrate, or the damage over a nano wire when it does not have sufficient reinforcement for a nano wire to support a soluble substrate (for example, when gravity

cannot be borne), the spacer which has desired thickness can also be used. A spacer can consist of thin films with a pattern beforehand deposited on the circuit board 10. Pattern attachment of the distribution of the nano wire 14 on the soluble substrate 22 can be carried out so that this nano wire may have consistency in the location of a contact pad. the catalyst nucleation thin film 26 (refer to drawing 2) with which this promotes growth of a nano wire for example, during CVD processing -- RISOGURAFU -- it can carry out by carrying out pattern attachment by law.

[0024] In drawing 5 C, it is in a condition [the soluble substrate 22 and that the catalyst nucleation thin film 26 will be removed if it exists, consequently the upper parts 16a, 16b, and 16c of a nano wire etc. are exposed], and a nano wire is joined to the circuit board 10. A nano wire can be further covered with a solder ingredient which was explained in relation to drawing 4 A - 4C. Thereby, as shown in drawing 5 D, the up exposure part of a nano wire can be again covered with solder 36'. a contact -- a pad -- 12 -- a -- ' -- 12 -- b -- ' -- having -- the circuit board -- ten -- ' -- from -- becoming -- doubling -- a device (refer to drawing 5 D) -- preparing -- and -- solder -- an ingredient -- a layer -- 38 -- ' -- a contact -- a pad -- 12 -- a -- ' -- 12 -- b -- ' -- a top -- it can also arrange . For example, a circuit device is contacted on an exposure nano wire by arranging to an upside-down, and doubling substrate 10' is arranged. Then, a substrate is heated, components are soldered together, and perpendicular interconnect is completed as shown in drawing 5 E. In order to use it for positioning a device perpendicularly before a soldered joint, a spacer or a minute positioning device electrode holder (not shown) can also be arranged on the circuit board 10 of one side or both, and 10'.

[0025] the upper part -- a device -- ten -- ' -- nano -- a wire -- the upper part -- 16 -- a -- 16 -- b -- 16 -- c -- joining -- a thing -- using it -- having -- solder -- an ingredient -- 36 -- ' -- 38 -- ' -- nano -- a wire -- the lower part -- a part (36 for example, 38) -- the lower part -- a device -- ten -- joining -- a thing -- using it -- having had -- a thing -- being the same -- an ingredient -- it can be . In this case, a lower soldered joint receives melting and a solidification process twice [at least]. As an exception method, a lower device is joined using the 1st solder ingredient, and an up device is joined using the 2nd solder ingredient which has low soldering temperature. If it does in this way, when up junction will be formed, lower junction does not receive melting and a solidification process. For example, in the case of a lower device, solder 36 and 38 consists of Au-Sn (for example, it has the melting point of about 280 degrees C) eutectic-mixture solder, and, in the case of an up device, on the other hand, solder 36' and 38' consist of Sn-Ag (for example, it has the melting point of about 215 degrees C) eutectic-mixture solder. As an exception method, the 1st solder ingredient 36 and 38 for lower devices can consist of Sn-Pb (for example, it has the melting point of about 183 degrees C) eutectic-mixture solder, and, on the other hand, 2nd solder ingredient 36' for up devices and 38' can also consist of Bi-Sn (for example, it has the melting point of about 139 degrees C) eutectic-mixture solder. Moreover, multilayer perpendicular interconnect of a device can also be formed using different solder which has melting point rank. Furthermore, in order to heighten the interface junction force between solder, a nano wire, or a circuit pad front face, a solder ingredient can also contain one or more kinds of carbide generation elements by the case.

[0026] The minute thing of the dimension of the nano wire used for formation of perpendicular interconnect is desirable. Generally, the diameter of each nano wire is less than about 200nm, is less than 50nm preferably, and is less than 10nm further much more preferably. Generally the height of each connection or the die length of each nano wire is within the limits of about 10-1000nm. It is at least 10nm desirably, and preferably, even if the die length of a nano wire does not have ****, it is 100nm and is at least 1000nm further much more preferably. Thereby, a nano wire is thin fully for a long time, although a high aspect ratio and mechanical comp rye ANSI are attained. However, restraint exists in extending a nano wire excessively. Especially in the case of a carbon nanotube, covering the overall length, an electrical property is maintained or it becomes much more difficult to maintain perpendicular alignment, so that a nano wire becomes long. Moreover, a long nano wire results in a long process. For example, in order to obtain the extended die length, growth must be made to continue for a long period of time. Generally, the upper limit of the die length of a nano wire is less than 100 micrometers, is less than 20 micrometers much more preferably, and is less than 2 micrometers further much more preferably.

[0027] Itself other than [with the direct nano wire used with the structure which interconnected perpendicularly] conductivity can also have a device property. For example, a compound nano wire can also have at least one heterojunction which exists along with the die length of a nano wire. A silicon semi-conductor nano wire can be grown up on the end of a metallicity carbon nanotube, or this reverse is also possible for it. For example, J.Hu et al., NATURE, Vol.399 (1999), p.48 reference. A metal-semi-conductor heterojunction can be included in one or more nano wires, and it can be used as a rectifier-diode device. The device of the type of others like p-n junction or the tunnel device structure is also incorporable into a nano

wire. Drawing 6 is the typical sectional view of the interconnect device with which the nano wire itself consists of complex of metallicity carbon nanotube 4a and semi-conductor wire 4b. The lower circuit board 10 has the contact pads 12a and 12b on the front face, and the nano wire is joined to the contact pad in the part which consists of carbon nanotube 4a. The upper part of nano wire 4b which up circuit board 10' has contact pad 12a' and 12b' on the front face, and consists of a semi-conductor wire is joined to these insulated-contact pad 12a' and 12b'. These compound nano wires can grow by the adjustment parallel-connected-type formula on a soluble substrate, and can make that die length able to isometry-ize as mentioned above, and can join this compound nano wire with solder to a substrate 10 and 10' as mentioned above. Array structure can be used for the high density assembly of such a device.

[0028] For example, the soluble substrate which is not based on the dissolution processing under an undissolved substrate or subsequent processing can be used instead of using a soluble substrate for initial growth of a nano wire. A substrate can join the other-end section to a desired circuit pad powerfully by soldered joint, while deducting mechanically and making it dissociate from the nano wire in the edge of a pair. When using an exception [this] method, the junction force in a substrate-nano wire interface must be more sharply [than the junction force in a nano wire-pad interface] low. For example, the carbon nanotube which grew on the quartz substrate has the comparatively low junction force, and can be made to separate it from a substrate easily by using weak mechanical power.

[0029]

[Effect of the Invention] As explained above, according to this invention, the circuit device which interconnected perpendicularly using the nano wire and such a nano wire of in general equal die length which can be formed as a suitable self-standing unit for convenient perpendicular interconnect can be obtained.

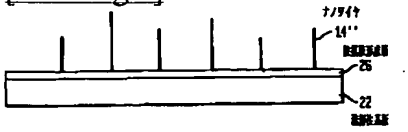
[Translation done.]

* NOTICES *

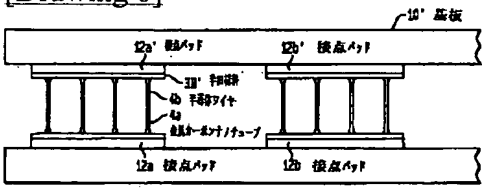
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

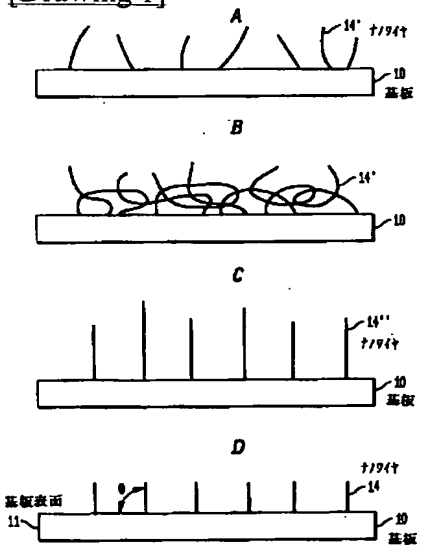
[Drawing 2]



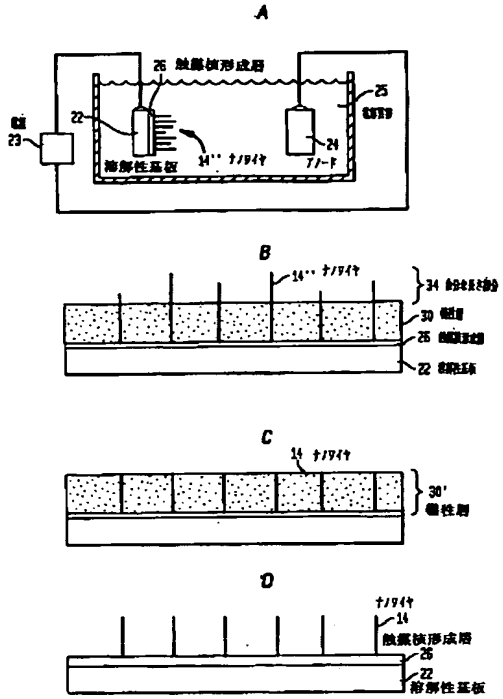
[Drawing 6]



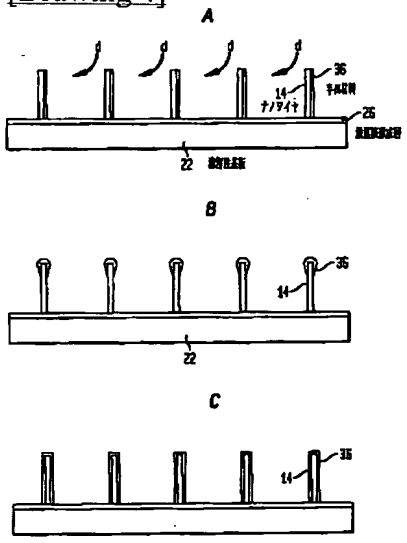
[Drawing 1]



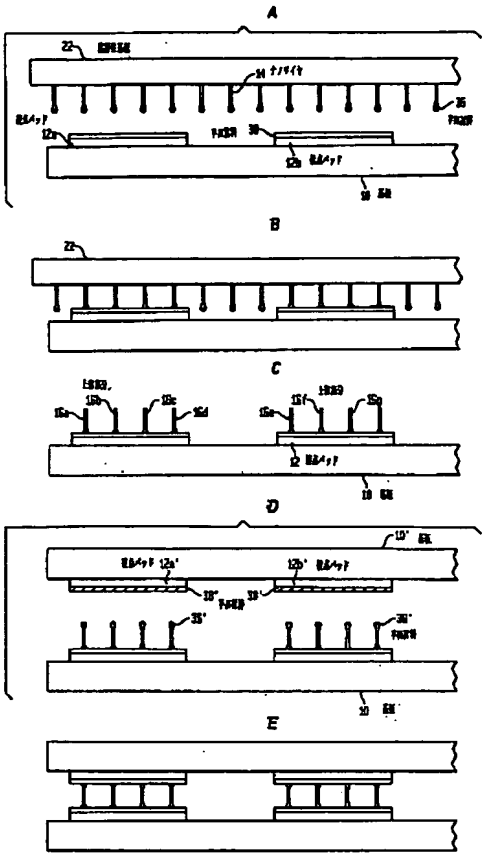
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2002－141633
（P2002－141633A）
(43)公開日　平成14年５月17日(2002.5.17)

(51)Int.Cl.⁷	識別記号	ＦＩ		テーマコード（参考）
Ｈ０５Ｋ　1/14		Ｈ０５Ｋ　1/14	Ｈ	４Ｇ０４６
Ｂ８２Ｂ　1/00		Ｂ８２Ｂ　1/00		４Ｋ０３０
3/00		3/00		５Ｅ３４４
Ｈ０１Ｌ　23/52		Ｈ０５Ｋ　3/36	Ｚ	
Ｈ０５Ｋ　3/36		Ｃ０１Ｂ　31/02	１０１Ｆ	

審査請求　未請求　請求項の数24　ＯＬ　外国語出願　（全 37 頁）　最終頁に続く

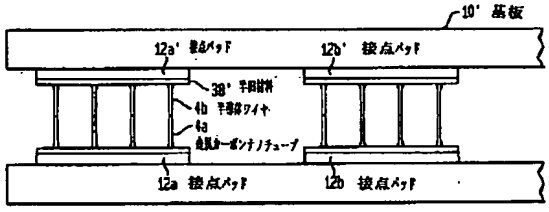
(21)出願番号　特願2000－324945(P2000－324945)
(22)出願日　平成12年10月25日(2000.10.25)

(71)出願人　596077259
ルーセント　テクノロジーズ　インコーポレイテッド
Ｌｕｃｅｎｔ　Ｔｅｃｈｎｏｌｏｇｉｅｓ　Ｉｎｃ.
アメリカ合衆国　07974　ニュージャージー、マレーヒル、マウンテン　アベニュー　600－700
(74)代理人　100064447
弁理士　岡部　正夫　（外12名）

最終頁に続く

(54)【発明の名称】　垂直にナノ相互接続された回路デバイスからなる製品及びその製造方法

(57)【要約】
【課題】　等長ナノワイヤ及び該ナノワイヤを用いて垂直に相互接続された回路デバイスを提供する。
【解決手段】　少なくとも２つの回路層と、該回路層間に配置された複数の等長ナノワイヤとを有する垂直に相互接続された回路デバイスにより解決される。ナノワイヤは、その長さに沿って存在するヘテロ接合を有する複合物からなり、多数のデバイス用途に使用できる。回路デバイスの製造方法は、(a)複数のナノワイヤを除去可能な基板上に成長させるステップと、(b)ナノワイヤの長さを均等化させ、複数のナノワイヤの各々の長さを概ね等しくするステップと、(c)移送し、複数のナノワイヤの露出端部を第１の回路層に接合させるステップと、(d)基板を除去するステップとからなる。第１の回路層に接合されたナノワイヤを第２の回路層へ更に接合させることにより垂直に相互接続された回路デバイスを形成できる。



1

【特許請求の範囲】

【請求項１】　少なくとも２つの回路層と、該少なくとも２つの回路層間に配置され、かつ、該少なくとも２つの回路層を電気的に相互接続する、複数の概ね等しい長さのナノワイヤとからなる回路デバイスを有することを特徴とする製品。

【請求項２】　前記複数のナノワイヤの各々の直径が５００ｎｍ未満である、ことを特徴とする請求項１に記載の製品。

【請求項３】　前記複数のナノワイヤの各々が概ね垂直に整列されている、ことを特徴とする請求項１に記載の製品。

【請求項４】　少なくとも２つの回路層と、垂直に配置され、かつ、該少なくとも２つの回路層を電気的に相互接続する複数の概ね平行で等しい長さのナノワイヤからなる回路デバイスを有し、前記複数のナノワイヤの各々の直径が５００ｎｍ未満であり、前記複数のナノワイヤの各々は、金属半田接合により、前記少なくとも２つの回路層のうちの一方に接合されていることを特徴とする製品。

【請求項５】　前記複数のナノワイヤは外部応力に関連する信頼性問題を避けるための機械的コンプライアンシーを示す、ことを特徴とする請求項４に記載の製品。

【請求項６】　前記複数のナノワイヤはカーボンナノチューブ、半導体ナノチューブ及び金属類、合金類、酸化物類、窒化物類、ホウ化物類又は混合セラミックスのうちの少なくとも１種類から形成されたナノワイヤからなる群から選択される、ことを特徴とする請求項４に記載の製品。

【請求項７】　前記ナノワイヤのうちの任意の１本の長さが前記複数のナノワイヤの全ての平均長さから２０％未満まで逸脱する、ことを特徴とする請求項４に記載の製品。

【請求項８】　前記複数のナノワイヤのうちの少なくとも１本は、その長さに沿って存在するヘテロ接合を有する複合ナノワイヤからなる、ことを特徴とする請求項４に記載の製品。

【請求項９】　(a)基板を準備するステップと、
(b)複数のナノワイヤの各々が第１の露出端部と、前記基板に結合された第２の端部とを有するように、複数のナノワイヤを前記基板上に成長させるステップと、
(c)前記複数のナノワイヤの各々の長さが概ね等しくなるように、前記ナノワイヤの長さを等長化させるステップと、
(d)前記複数のナノワイヤの前記第１の露出端部を第１の回路層に接合させるステップと、
(e)前記複数のナノワイヤの第２の端部が露出したまま、前記第１の回路層に接合された前記複数のナノワイヤを有する回路デバイスを形成するために、前記基板を除去するステップとからなる、ことを特徴とする回路デバイスの製造方法。

2

【請求項１０】　前記基板除去ステップは、前記複数のナノワイヤの第２の端部を前記基板から機械的に分離することからなる、ことを特徴とする請求項９に記載の方法。

【請求項１１】　前記基板は溶解性基板からなり、前記基板除去ステップは、前記基板を化学的に溶解することからなる、ことを特徴とする請求項９に記載の方法。

【請求項１２】　(f)第２の回路層を準備するステップと、
(g)前記複数のナノワイヤの第２の露出端部を第２の半田材料で被覆するステップと、
(h)垂直に相互接続された回路デバイスを形成するために、前記第２の露出端部を前記第２の回路層に接合させるステップとを更に有する、ことを特徴とする請求項９に記載の方法。

【請求項１３】　前記複数のナノワイヤの成長ステップは、触媒核形成層を前記溶解性基板上に被着させ、前記触媒核形成層に隣接したガスを分解することからなる、ことを特徴とする請求項９に記載の方法。

【請求項１４】　前記ガスは、カーボンナノチューブが前記溶解性基板上で成長するように、炭化水素含有ガスからなる、ことを特徴とする請求項１３に記載の方法。

【請求項１５】　(i)前記複数のナノワイヤの第１及び第２の露出端部のうちの少なくとも一方に半田材料を被覆するステップを更に有する、ことを特徴とする請求項９に記載の方法。

【請求項１６】　前記半田材料を、蒸着により、前記複数のナノワイヤの第１及び第２の露出端部のうちの少なくとも一方に塗布し、その際、前記半田材料の前記複数のナノワイヤへの均一塗布を促進するために、前記溶解性基板を回転させる、ことを特徴とする請求項１５に記載の方法。

【請求項１７】　前記第１及び第２の回路層は各々、複数の接点パッドを有し、半田材料層を前記第１及び第２の回路層上の各接点パッドに塗布し、前記複数のナノワイヤの第１及び第２の端部を前記接点パッドへ接合させる、ことを特徴とする請求項１５に記載の方法。

【請求項１８】　前記第１の露出端部を前記第１の回路層へ接合させるために使用される第１の半田材料は第１の半田付け温度を有し、前記第２の露出端部を前記第２の回路層へ接合させるために使用される第２の半田材料は第２の半田付け温度を有し、前記第２の半田付け温度は前記第１の半田付け温度よりも低い、ことを特徴とする請求項１７に記載の方法。

【請求項１９】　前記ナノワイヤの長さを等長化させるステップは、
(i)前記溶解性基板に結合された前記複数のナノワイヤを概ね均一な厚さの犠牲材料層中に部分的に埋め込み、それによりナノワイヤの余分な長さ部分を前記犠牲材料

から突出させるステップと、
(ii)前記ナノワイヤの余分な長さ部分を除去するステップと、
(iii)前記犠牲材料を除去するステップとからなる、ことを特徴とする請求項９に記載の方法。
【請求項２０】　前記犠牲材料層の前記溶解性基板への接着力を高めるために使用される、前記溶解性基板と前記触媒核形成層との間に間挿された導電性下地層を更に有する、ことを特徴とする請求項１９に記載の方法。
【請求項２１】　前記犠牲材料は電気メッキにより被着される、ことを特徴とする請求項１９に記載の方法。
【請求項２２】　前記犠牲材料層の厚さは約１～１００μｍの範囲内である、ことを特徴とする請求項１９に記載の方法。
【請求項２３】　前記複数のナノワイヤの平均直径は２００ｎｍ未満であり、半導体ｐ－ｎ接合及びトンネル接合のうちの少なくとも一方を含有する、ことを特徴とする請求項１に記載の製品。
【請求項２４】　請求項１による垂直に相互接続されたナノワイヤ整流ダイオードデバイスのアレーからなる製品。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明はナノ相互接続された又はナノパッケージされた回路を製造する構造物及びその製造方法に関する。更に詳細には、本発明は導電性ナノワイヤを用いた垂直電気接続に関する。
【０００２】
【従来の技術】直径が１～１００ナノメータ、長さが０．１～１００μｍ程度の非常に微小なサイズスケールを有するカーボンナノチューブのようなナノスケールワイヤは最近、大きな注目を浴びている。このようなナノスケールワイヤは例えば、Liu etal., SCIENCE, Vol. 280, p. 1253 (1998); Ren et al., SCIENCE, Vol. 282, p. 1105 (1998); Lie et al., SCIENCE, Vol. 274, p. 1701 (1996); Frank etal., SCIENCE, Vol. 280, p. 1744 (1998); J. Tans et al., NATURE, Vol. 36,p. 474 (1997); Fan et al., SCIENCE, Vol. 283, p. 512 (1999); Collins etal., SCIENCE, Vol. 278, p. 100 (1997); Kong et al., NATURE, Vol. 395, p. 878 (1998); 及びEbbensen et al., NATURE, Vol. 382, p. 54 (1996)などに記載されている。
【０００３】カーボンナノチューブは独特な原子配列、ナノスケール構造及び興味深い物理的性質（例えば、一次元的な電気的挙動、量子コンダクタンス及び衝撃輸送特性など）を示す。Frankらにより報告されているように、カーボンナノチューブにおける衝撃輸送は、幾つかの超伝導体における電流密度に匹敵するか又は凌駕する大きさの電流密度で、電子回路内を巨大な電流が通過することを可能にする。カーボンナノチューブは最小寸法のナノワイヤ材料の一例であり、一般的に、高アスペクト比と、単壁ナノチューブの場合には～１ｎｍの小さな直径を有し、多壁ナノチューブの場合には～５０ｎｍ未満の直径を有する。これらについては、Rinzler et al, APPLIED PHYSICS, Vol. A67, p. 6612 (1994)及びKiang et al,PHYSICAL REVIEW LETTERS, Vol. 81, p. 1869 (1998)に記載されている。
【０００４】高品質の単壁カーボンナノチューブは一般的に、レーザ・アブレーション又はアーク技術により、ランダムな方向に、針状又はスパゲッティ状のもつれたナノチューブとして成長する。（黒鉛又はアモルファス相、触媒金属などのような非ナノチューブ物質を除去するために、アーク技術による生成されたカーボンナノチューブについては一般的に、化学的な精製処理が必要である。）Renら、Fanら及びLiらにより使用されたような化学的気相成長（ＣＶＤ）法は、基板に付着した多壁ナノチューブを生成する傾向がある。この場合、しばしば、基板に対して垂直な、半整列又は整列されたパラレル成長を示す。これらの文献に記載されているように、温度、時間、先駆体濃度、流量などのような反応パラメータが最適化されると、エチレン、メタン又はベンゼンなどのような炭化水素含有先駆体の触媒分解によりカーボンナノチューブが生成される。Ｎｉ、Ｃｏ、Ｆｅの錫被膜のような核形成層はしばしば意図的に基板表面に追加され、様々な単離ナノチューブを核形成する。また、カーボンナノチューブは、前記のような金属核形成層を使用することなく、１種類以上のこれらの触媒金属原子を含有する化学成分（例えば、フェロセン）と混合された炭化水素含有先駆体を使用することにより、基板上に核形成させ、かつ成長させることもできる。化学的気相成長中に、これらの金属原子は基板面へのナノチューブの核形成を促進する。これについては、Cheng et al., CHEM. PHYSICS LETTERS, Vol. 289, p. 602 (1998)に記載されている。
【０００５】電子回路設計、相互接続及びパッケージングにおける最近の傾向は一層微細なフィーチャー(feature)を使用する方向に向かっている。このようなサブミクロンフィーチャーサイズはつい最近になって到達したサイズである。所望の超高密度電子パッケージングを生成するために、垂直に集積された回路層を有する３次元多層形状と同様に、微小な線幅の回路ラインが重要である。しかし、現在利用可能な方法により成長されたナノワイヤはこのような目的には不適当である。レーザ・アブレーション又はアーク技術により一般的に合成されたような成長したままの単壁ナノチューブ（ＳＷＮＴ）はスパゲッティ状の形状を有し、しばしば互いにもつれあっている。化学的気相成長法により一般的に形成されたような多壁ナノチューブ（ＭＷＮＴ）は一層簡単に、整列されたパラレル形状に生成することができる。しかし、Renら及びLiらにより報告されたような、これらの

成長したままのナノチューブは高さ又は長さが異なる。電気的短絡又は開放の無い高信頼性の回路相互接続の場合、等しい所定の長さを有するナノチューブを生成することが望ましい。更に、自立性ワイヤとしてナノチューブを形成することが好都合である。その結果、これらのナノチューブは例えば、室温又は比較的低い温度（例えば、３００℃以下）における回路相互接続のための、移送、配置及びボンディングなどについて精巧に操作することができる。所望の回路パッド上に直接に成長されたカーボンナノチューブのようなナノチューブの選択的なＣＶＤ成長は、触媒層の選択的なエリアパターニングを用いて実施することができる。しかし、大抵の場合、デリケートな半導体回路及びコンポーネントを高温（例えば、６００～１０００℃）及びナノチューブのＣＶＤ析出に伴う化学環境に暴露することは望ましくない。

【０００６】

【発明が解決しようとする課題】従って、本発明の目的は、便利な垂直相互接続に好適な自立性ユニットとして形成することができる概ね等しい長さのナノワイヤ及びこのようなナノワイヤを用いて垂直に相互接続された回路デバイスを提供することである。

【０００７】

【課題を解決するための手段】前記課題は、少なくとも２つの回路層と、該回路層間に配置された複数の概ね等しい長さのナノワイヤとを有する垂直に相互接続された回路デバイスにより解決される。本発明のナノワイヤは、例えば、その長さに沿って存在するヘテロ接合を有する複合物からなり、多数のデバイス用途に使用できる。また、本発明の回路デバイスの製造方法は、(a)複数のナノワイヤを除去可能な基板上に成長させるステップと、(b)ナノワイヤの長さを均等化させる（例えば、その結果、複数のナノワイヤの各々の長さが概ね等しくなる）ステップと、(c)移送し、そして複数のナノワイヤの露出端部を第１の回路層に接合させるステップと、(d)基板を除去するステップとからなる。第１の回路層に接合されたナノワイヤを、第２の回路層へ更に接合させることにより垂直に相互接続された回路デバイスを形成することができる。

【０００８】

【発明の実施の形態】本発明はカーボンナノチューブのような導電性のナノワイヤの製造方法に関する。このカーボンナノチューブは、回路デバイス層間の、ナノスケールの垂直接合用ワイヤとして、かつ、隣接する電気的接点パッド間の平面内の接続ワイヤとして有用である。２つの回路層間又は嵌合デバイスのような回路相互接続の場合、多数の細分されたパラレル導電パスの使用は整列されたナノワイヤにより達成される。ナノワイヤは、例えば、望ましからざる応力により発生する短期信頼性及び長期信頼性問題を避けるのに好都合な相互接続媒体の弾性コンプライアンス及び柔軟性を提供する。相互接続媒体に長期にわたって持続的に加えられる共通応力源は例えば、局所温度勾配、デバイス内で使用されている異なる材料間の熱膨張率のミスマッチにより生起する応力、電子泳動誘発性応力及びデバイスの組み立て、取り扱い、試験又は輸送中に導入される機械応力及び熱応力などである。本発明によれば、相互接続媒体又は回路部品の疲労、クリープ又は変形破損などのような応力により生起される信頼性問題を避けるか又は最小化することができる。微小直径のナノワイヤを使用する場合、本発明は高密度又は超高密度回路相互接続を達成するのに有用である。

【０００９】図１Ａ～１Ｄは、基板１０上に成長された様々な形状のナノワイヤの模式図である。ナノワイヤは、カーボンナノチューブ、例えば、Ｓｉ、Ｇｅ又はＧａＡｓにより形成された半導体ナノワイヤ又は金属類、合金類、酸化物類、カーバイド類、窒化物類、ホウ化物類若しくは混合セラミック類などのような当業者に公知のその他の導電性又は非導電性材料から形成されたナノワイヤから構成することができる。ナノワイヤの製造方法は、レーザ・アブレーション、アーク放電又は先駆体ガス若しくは先駆体ガス混合物の化学的気相成長などからなる。微小直径ナノワイヤは、気相の触媒分解により核形成し、そして基板から上方へ成長させることができる。この場合、触媒薄膜を基板上に蒸着し、この薄膜の局所核形成を気相中で触媒分解することにより開始させる。例えば、ガラス回路基板を準備し、遷移金属からなる触媒薄膜をガラス基板上に蒸着し、次いで、この薄膜基板上でC_2H_4を分解することによりカーボンナノチューブを形成することができる。この触媒薄膜はこの明細書において触媒核形成薄膜とも呼ばれ、この薄膜はＮｉ、Ｃｏ又はＦｅ若しくは当業者に公知のその他の材料から構成することができる。

【００１０】整列処理が無い場合、ナノワイヤは図１Ａ及び図１Ｂにそれぞれ示されるように、ランダムな方向に向かって成長したり或いは縺れ（もつれ）合うように成長しやすい。ナノワイヤ１４’のもつれた形態（図１Ｂ）はレーザ・アブレーションの使用によっても得られる。しかし、垂直相互接続において都合良く使用するには、ナノワイヤは概ね垂直に整列されていることが好ましい。例えば、印加電界、ガス濃度勾配又は温度勾配の使用により、ナノワイヤが形成されるに応じて、ナノワイヤを整列させることができる。また、基板中の凹陥垂直キャビティを使用する物理的技法により又は密集化（例えば、ナノワイヤの“密林”（例えば、単位面積当たりの高濃度）の同時形成）により成長させるに応じてナノワイヤを整列させることができる。ナノワイヤの整列成長を促進させるために、触媒核形成薄膜と共に、多孔質セラミック又はシリコン層を併用することもできる。図１Ｃに示されるように、整列ナノワイヤは不均一な長さ１４”であるか、又は図１Ｄに示されるように、

均一な長さ１４であることができる。図１Ｄに示されるような態様、すなわちナノワイヤが概ね整列され、かつ、概ね等しい長さであるような態様が好ましい。各ナノワイヤの長さは平均ナノワイヤ長さから２０％未満まで、一層好ましくは１０％未満までしか変動しないことが好ましい。

【００１１】ナノワイヤ１４は基板に対して垂直に整列され、かつ、概ね並列に配列されていることが好ましい。ナノワイヤの完全に垂直な整列（例えば、図１Ｄに示されるように、基板の表面１１とナノワイヤの長さとの間の角度φが９０°であること）は不要である。しかし、完全垂直整列からの変動は微小であることが好ましい。すなわち、この変動は完全垂直（９０°）整列から約２５°未満、好ましくは１５°未満である。

【００１２】垂直相互接続の形成における使用を容易化するために、ナノワイヤを溶解可能な別の基板上に成長させることができる。例えば、図２は、触媒核形成薄膜２６を使用して成長された、溶解性基板２２上の不均一な長さの垂直整列ナノワイヤ１４”を示す。溶解性基板は下記で説明するように、回路相互接続の形成におけるナノワイヤの移転を手助けする。溶解性基板層は水、酸、塩基又は溶剤に溶解させることができる。例えば、塩化ナトリウム結晶を使用し、水溶性基板を形成することができる。酸溶解性基板を形成するには、Ｃｕ、Ｎｉ、Ｃｏ、Ｍｏ、Ｆｅ、Ｖ、Ａｕ、Ａｇ又はこれらの合金類などのような金属類を使用することができる。塩基溶解性基板を形成するには、Ａｌのような金属類を使用することができる。例えば、ＣＶＤ法によるナノワイヤ成長温度が、使用される基板材料の融点以下となるように、基板を選択しなければならない。別法として、別の基板層を形成するために溶解性ポリマー材料を使用することもできる。このようなポリマー材料は、ポリビニルアルコール、ポリビニルアセテート、ポリアクリルアミド、アクリロニトリル・ブタジエン・スチレン又は揮発性物質（例えば、ポリメチルメタクリレート（ＰＭＭＡ））などである。ポリマーを使用する場合、ナノワイヤの処理において使用される温度は、分解、物理形状の変化又は化学特性の変化などのようなポリマーの損傷を避けるために、十分に低い温度でなければならない。材料を併用することによっても溶解性基板層を形成することもできる。ナノワイヤを成長させるために、溶解性基板に触媒核形成薄膜２６（例えば、Ｎｉ、Ｆｅ又はＣｏ）を被覆することもできる。ナノワイヤが成長された後、溶解性基板を除去することができる。触媒核形成薄膜は例えば、スパッタリング、蒸着又は電気化学メッキにより連続層として若しくはスポット的又はパターン的形態で、溶解性層上に堆積させることができる。

【００１３】図１Ｃ及び図２に示されるように、ナノワイヤは最初、不均一な長さに成長させ、次いで、等長化処理を施すことにより、図１Ｄに示されるように、概ね等しい長さのナノワイヤを形成することができる。前記のように、等しい長さのナノワイヤが好ましい。このことは例えば、米国特許出願第０９／３５４９２８号明細書に記載されている。等長化方法の一例は図３Ａ～図３Ｄに模式的に図示されている。この実施例における等長化方法は概ね３つのステップからなる。すなわち、(1)不均一な長さのナノワイヤを概ね均一な厚さの溶解性犠牲層３０内に埋め込むステップ（図３Ａ～３Ｂ）と、(2)犠牲層から突き出ているナノワイヤの余分な長さ３４を除去するステップ（図３Ｃ）と、(3)犠牲層を除去するステップ（図３Ｄ）とからなる。言うまでもなく、レーザ切断及びホットブレード切断などのようなその他の等長化方法も使用できる。これについては、米国特許出願第０９／２３６９３３号明細書に記載されている。

【００１４】図３Ａ～３Ｄの実施例における方法では、第１のステップは、概ね均一な厚さの犠牲層を堆積させることである。図３Ａは、電気メッキ装置及び不均一な長さのナノワイヤ１４”を有する基板２２上に犠牲層３０を堆積させる方法を示す。この実施例では、銅（Ｃｕ）溶解性基板層２２を準備し、この基板層上に膜厚が約１～１００ｎｍのニッケル（Ｎｉ）からなる触媒核形成薄膜２６を堆積させる。言うまでもなく、前記のようなその他の材料も溶解性基板層２２又は核形成薄膜２６のために使用できる。図３Ａでは、触媒核形成薄膜２６は連続層として図示されている。しかし、触媒核形成薄膜は（例えば、連続層として堆積されている場合であっても）、例えば、化学的気相成長及びナノワイヤ成長において加熱されたときに、断片状又は島状に破断されることがある。触媒核形成薄膜のこのような断片化は、導電性金属膜を被せることなく、減少されたナノワイヤ間に溶解性基板の表面を残す。溶解性基板を構成する材料に応じて、基板及び断片化触媒核形成薄膜に金属犠牲層３０を被覆することが困難なことがある（図３Ｃ、下記で説明する）。これは、例えば、溶解性基板が絶縁性である（例えば、塩化ナトリウムから構成されている）ような場合である。従って、触媒核形成薄膜を堆積させる前に、溶解性基板上に先ず非触媒性導電性下地層（図示されていない）を堆積させることができる。換言すれば、図２において、溶解性基板２２と触媒核形成薄膜２６との間に下地層を間挿させることができる。この下地層はＭｏ又は当業者に公知のその他の非触媒性導電性材料から構成することができる。

【００１５】Ｃｕ基板層２２は、この方法においてはカソードとして機能し、アノード２４（例えば、ニッケルアノード）に隣接し、電源２３によりアノードに結合された電解質浴２５内に配置されている。電解質２５は堆積されるべき金属のイオンを含有している。例えば、$NiSO_4$含有溶液からＮｉを堆積させるか又は$CuSO_4$溶液からＣｕを堆積させる。電解質浴２５は、触媒核形成薄膜２６又は導電性下地層のイオンと同じタイプのイ

オンを含有していることが好ましい。このようにして、化学親和力により、犠牲層３６の電気メッキは、ナノワイヤ１４”（例えば、カーボン又はシリコンナノワイヤ）上にではなく、触媒核形成薄膜２６の表面上で起こる。例えば、犠牲層３０は触媒核形成薄膜と同じ金属特性を有し、ナノワイヤとは大幅に異なる特性を有する。犠牲層は、ナノワイヤの所望の長さと概ね同じ膜厚にまで堆積される。このパラメータ（ナノワイヤ長さ）は所望のセンサの適用に応じて変化するが、一般的に、前記のように１～１００ｎｍの範囲内である。犠牲層の膜厚は、時間、電解質濃度、電流密度などのような作業変数により制御することができる。言うまでもなく、図３Ａは犠牲層を堆積する方法の一例を示すだけである。犠牲層は、無電解メッキ、化学的気相成長又は物理蒸着（例えば、スパッタリング、蒸着、レーザ・アブレーション又はイオンビーム蒸着）のようなその他の方法によっても堆積させることができる。

【００１６】図３Ｂは図３Ａの電気メッキ方法により得られた構造物の断面図である。この構造物は、溶解性基板層２２、触媒核形成薄膜２６、概ね均一な膜厚の犠牲層３０内に埋め込まれた不均一な長さのナノワイヤ１４”からなる。各ナノワイヤ１４”は犠牲層３０を超えて突出する露出された余分な長さ部分３４を有する。余分な長さ部分３４が除去される際、犠牲層３０は埋没ナノワイヤを一時的に保護する。犠牲層は容易に除去可能な材料から構成されていることが好ましい。このような材料は例えば、犠牲層を水又は溶剤に溶解させることにより除去可能であるような材料、化学エッチング又は電気化学エッチングにより除去可能であるような材料又は加熱により気化させることにより除去可能であるような材料などである。好適な水溶性又は溶剤可溶性材料は例えば、塩化ナトリウム、塩化銀、硝酸カリウム、硫酸銅及び塩化インジウムのような塩類又は砂糖及びグルコースのような有機物類などである。化学的にエッチング可能な好適材料は例えば、Ｃｕ、Ｎｉ、Ｆｅ、Ｃｏ、Ｍｏ、Ｖ、Ａｌ、Ｚｎ、Ｉｎ、Ａｇ、Ｃｕ－Ｎｉ及びＮｉ－Ｆｅのような金属類及び合金類などである。これらの材料から形成された犠牲層は、塩酸、王水又は硝酸のような酸又は水酸化ナトリウム又はアンモニアのような塩基性溶液で溶解除去させることができる。好適な気化可能材料は例えば、Ｚｎのような高蒸気圧を示す材料又は有機酸類のような適当な酸化、還元又は天然ガス雰囲気中で加熱処理することにより分解又は焼却させることができる材料などである。

【００１７】等長化方法の次のステップは、図３Ｃに示されるように、ナノワイヤの露出部分３４を除去し、犠牲層３０内に埋め込まれた等長ナノワイヤ１４を得ることからなる。この除去作業は例えば、化学的又は機械的方法により露出部分３４を研磨あるいはエッチングすることにより実施できる。カーボンナノワイヤが使用されている場合、露出部分の除去には、加熱処理を使用することもでき、この加熱は好ましい処理方法である。例えば、余分な長さ部分３４は、この構造物を例えば、２００℃～１０００℃の範囲内の温度で、酸化雰囲気中で加熱することにより除去することができる。完全な又は部分的な酸素若しくはオゾン雰囲気を使用できる。別法として、ナノワイヤの余分な長さ部分を除去するために、機械的研磨処理法も使用できる。次のステップにおいて、等長ナノワイヤを有する犠牲層３０’（図３Ｃ参照）を、例えば、溶解させることにより除去する。このようにして、図３Ｄに示されるような、基板２２と、触媒核形成薄膜２６と概ね等しい長さのナノワイヤ１４を有する構造物が得られる。

【００１８】犠牲層３０’を除去する際、触媒核形成薄膜２６は溶解性基板２２の上に残らなければならない。なぜなら、触媒核形成薄膜２６が残らないと、ナノワイヤが基板２から分離してしまうからである。犠牲層が塩化ナトリウム、硫酸銅又はポリビニルアルコールのような非金属層からなる場合、触媒核形成薄膜を無傷のまま残した状態で、犠牲層を除去することができる。しかし、犠牲層が金属層からなる場合、酸エッチングによるような犠牲層の除去は、触媒核形成薄膜も除去してしまい、その結果、ナノワイヤが基板から分離されてしまう。この問題を処理するために、犠牲層を部分的（例えば、元の膜厚の半分又は１／３）にエッチングし、ナノワイヤの露出部分を回路デバイスに接続するのに十分な長さのナノワイヤを露出させる。この場合、例えば、溶解性基板及び触媒核形成薄膜を除去するときに、残りの犠牲層を事後的に除去することができる。中間処理ステップにおいて、例えば、変形、溶解などから溶解性基板を保護するために、この溶解性基板を仮保護層（図示されていない）で被覆することが好ましい。この仮保護層は溶解性基板の背面及び／又は側面に塗布することができる。この仮保護層は、溶剤（例えば、アルコール又はアセトン）で容易に除去されるが、水溶液には安定なラッカータイプの材料からなる。可溶性基板２２，触媒核形成薄膜２６及び犠牲層３０を構成する材料は、十分に異なるエッチング速度又は除去速度を有するように選択される。これにより、犠牲層の除去により触媒核形成薄膜が溶解されることを避け、及び／又は処理中に溶解性基板が損傷されることを避けることができる。

【００１９】例えば、図３Ｄに示されるような、溶解性基板により保持された等長並列ナノワイヤは、垂直ナノスケール回路相互接続及びタクチックセンサーデバイスなどの様々なデバイス用途にとって有用である。或る用途については、ナノワイヤの少なくとも一部分に、電気的に導電性であり、かつ好ましくは接合可能（半田付け可能）金属又は合金の薄膜又は被膜３６（図４Ａ～４Ｃ参照）を塗布することができる。場合により、接着促進層（図示されていない）を、被膜３６とナノワイヤ１４

との間に配設することもできる。ナノワイヤのメタライジング処理は、ナノワイヤの長さ方向に沿って導電性を確保するのに有用である。被膜３６はナノワイヤの少なくとも一部に塗着することができる。被膜３６は、導電性であり、かつ好ましくは接合可能な（半田付け可能な）金属又は合金の薄膜からなる。被膜３６は例えば、Ａｕ、Ａｇ、Ｐｄ、Ｒｈ、Ｎｉ、Ｃｕ、Ｉｎ又はＳｎのような半田付け可能な金属薄膜又はＡｕ－Ｓｎ、Ｓｎ－Ａｇ、Ｐｂ－Ｓｎ、Ｂｉ－Ｓｎ、Ｉｎ－Ｓｎ又はＩｎ－Ａｇのような半田合金薄膜である。カーボンナノチューブ又は窒化物タイプのナノワイヤの場合、被膜とナノワイヤとの間の接着促進中間層はカーバイド又は窒化物生成元素（例えば、Ｔｉ、Ｍｏ、Ｎｂ、Ｖ、Ｆｅ、Ｗ、Ｚｒ）から構成することができる。半田付け可能層及び接着促進層は多数の処理方法によりナノワイヤ表面に付加させることができる。このような処理方法は例えば、物理的蒸着法（スパッタリング、蒸着、イオンビーム蒸着）、化学的気相成長法、無電解電着、電気メッキ又は堆積方法の組合せなどである。別法として、接着促進元素を、合金元素として半田又は半田付け可能皮膜層自体の中に事前に添合させておくこともできる。ナノワイヤ表面と堆積接着促進層との間又は接着促進層と半田付け可能層との間の接着力を更に高めるために、随意の接着力向上加熱処理を加えることもできる。このような加熱処理は例えば、不活性又は真空雰囲気中で約１００～９００℃で０．１～１００時間加熱することからなる。

【００２０】図４Ａ～４Ｃは、様々な方法により塗布された金属被膜３６を示す概要断面図である。例えば、図４Ａは物理蒸着法により金属原子を照準線蒸着させた状態を示す。この蒸着は、金属がナノワイヤの一方の側に集中するように、例えば、矢線“ｄ”に従って、横方向に沿って行われる。ナノワイヤの表面全体にわたって一層均一に蒸着させるには、例えば、蒸着中に基板を回転させることによる変法により得ることができる。金属を堆積させる電気化学方法（例えば、電解メッキ又は無電解メッキ）は、図４Ｂに示されるように、選択的に局在化された堆積層を形成することができる。この選択的堆積は、ナノワイヤの先端付近の概して高い電解質濃度により生起させることができる。ＣＶＤ処理法により不均一プロファイルも得られる。被膜の均一性は様々な加工パラメータに応じて変化する。このようなパラメータは例えば、金属イオンが移動する速度、気体原子の堆積部位への移動及び被膜が堆積される速度などである。緩慢で、かつ一層細心に制御された堆積により、図４Ｃに示されるように、ナノワイヤの長さに沿って概ね均一な金属被膜３６を得ることができる。金属層又は半田付け可能層及び中間接着促進層（必要に応じて）の所望の膜厚は一般的に、０．５～５０ｎｍの範囲内であり、１～２０ｎｍの範囲内であることが好ましい。

【００２１】ナノワイヤに被覆された金属被膜は幾つかの重要な機能を果たす。

(1)金属被膜は回路基板にナノワイヤを接合させるための半田付け可能性を付与する。半田付け可能金属又は半田合金被膜は望ましくは、ナノワイヤに接合させるべき電気接点パッドの表面にも付加される。

(2)金属被膜は特に非金属ナノワイヤ、例えば、半導体カーボンナノチューブ、半導体ナノワイヤ（例えば、Ｓｉ又はＧａ－Ａｓ）又は絶縁ナノワイヤ（例えば、Al_2O_3、SiO_2、ＢＮ）若しくはその他の絶縁セラミックナノワイヤに均一な導電率を付与する。効率的で、高信頼性の垂直相互接続を形成する場合、ナノワイヤの長さを介して、下部回路デバイスに結合されるナノワイヤの一端から、上部デバイス又は上部回路層に接合されるナノワイヤの他端までの安定な電気的連続性が重要である。単壁ナノチューブは、炭素原子の“アームチェアー”形状を有する金属性であるか、又は“ジグザグ”タイプの形状若しくは或る種の“キラル”形状の半導体～略絶縁性であることができる。Dresselhous et al.,Science of Fullerines and Carbon Nanotubes, Chap. 19 (Academic Press, San Diego 1996), pp.･758, 805-809参照。ナノチューブ原子配列及び電気特性は単一カーボンナノチューブの長さに沿って劇的に変動することが知られている。Collins et al., SCIENCE, Vol. 278, p. 100 (Oct. 3, 1997)参照。このような電気特性の変動は、カーボンナノチューブ相互接続媒体を介するナノ相互接続デバイス間の効率的な電子輸送に悪影響を及ぼす。前記のようなナノワイヤ上の金属表面被膜はこの問題点を解決し、垂直ナノ相互接続媒体に所望の導電率を付与する。

(3)環境又は処理雰囲気に暴露されたときに、この金属被膜は半田付け可能被膜に対し耐食性／耐酸化性も付与し、更に、ナノワイヤが腐食／酸化を受けやすい場合にはナノワイヤ自体に対しても耐食性／耐酸化性を付与する。Ａｕ、Ａｇ、Ｐｄ、Ｒｈなどのような貴金属薄膜は被膜自体としても使用できるし或いはナノワイヤに被着された半田付け可能金属被膜３６の上面への追加上塗りとしても使用できる。Ａｕのような貴金属の薄い上塗りは半田付け処理中に、下部の溶融半田（例えば、Ａｕ－Ｓｎ又はＰｂ－Ｓｎ共融混合物半田）内に容易に吸収させることができ、その結果、接合を妨害しない。

【００２２】図５Ａ～５Ｅは、ナノワイヤを基板に接合させ、垂直相互接続を形成する方法の一例を例証する模式図である。図５Ａに示されるように、半田付け可能金属被膜が被覆された概ね等しい長さのナノワイヤ１４を有する溶解性基板２２を逆さまに配置する。接点パッド１２ａ、１２ｂを有する回路基板１０をナノワイヤと対面させるように配置する。接点パッドの形成用に使用される材料は例えば、Ａｌ、Ｃｕ、Ｗ、Ｔａ、ＴｉＮ、ＴａＮ、$CoSi_2$のような半導体回路製造で一般的に使用されている、多数の異なる導電性材料類から選択でき

る。場合により、追加の表面導電性被膜を使用することもできる。また、接点パッドには半田付け可能層３８を被覆することが好ましい。接点パッド１２ａ、１２ｂ等の面積は一般的に、２５μm^2未満であり、好ましくは１μm^2未満であり、一層好ましくは０．０１μm^2未満である。

【００２３】図５Ｂにおいて、ナノワイヤは接点パッドに物理的に接触した状態にされ、そして、その表面を加熱し、ナノワイヤを接点パッドに半田接合させる。ナノワイヤが溶解性基板を支持するのに十分な強度を有しない場合（例えば、重力に耐えられない場合）、基板の重量によるナノワイヤの潰れ又はナノワイヤに対する損傷を避けるために、所望の厚さを有するスペーサを使用することもできる。スペーサは回路基板１０上に予め堆積されたパターン付き薄膜から構成することができる。溶解性基板２２上のナノワイヤ１４の分布は、該ナノワイヤが接点パッドの位置に整合するように、パターン付けすることができる。これは例えば、ＣＶＤ処理中にナノワイヤの成長を促進する触媒核形成薄膜２６（図２参照）をリソグラフ法でパターン付けすることにより実施できる。

【００２４】図５Ｃにおいて、溶解性基板２２及び存在すれば触媒核形成薄膜２６が除去され、その結果、ナノワイヤの上部部分１６ａ，１６ｂ，１６ｃなどは露出されたままの状態で、ナノワイヤが回路基板１０に接合される。ナノワイヤは、例えば図４Ａ～４Ｃに関連して説明したような半田材料で更に被覆することができる。これにより、図５Ｄに示されるように、ナノワイヤの上部露出部分を半田３６’で再度被覆することができる。接点パッド１２ａ’，１２ｂ’を有する回路基板１０’からなる合せデバイス（図５Ｄ参照）を準備し、かつ半田材料層３８’を接点パッド１２ａ’，１２ｂ’上に配設することもできる。合せ基板１０’を例えば、回路デバイスを逆さまに配置することにより、露出ナノワイヤと接触させて配置する。その後、基板を加熱し、部品を一緒に半田付けし、図５Ｅに示されるように、垂直相互接続を完成させる。半田接合の前にデバイスを垂直に位置決めするのに使用するために、スペーサ又は微小位置決めデバイスホルダー（図示されていない）を一方又は両方の回路基板１０，１０’上に配置することもできる。

【００２５】上部デバイス１０’をナノワイヤの上部部分１６ａ，１６ｂ，１６ｃに接合するのに使用される半田材料３６’，３８’は、ナノワイヤの下部部分（例えば、３６，３８）に下部デバイス１０を接合するのに使用されたものと同じ材料であることができる。この場合、下部半田接合は少なくとも２度、溶融及び固化工程を受ける。別法として、第１の半田材料を使用して下部デバイスを接合し、低い半田付け温度を有する第２の半田材料を用いて上部デバイスを接合する。このようにすれば、上部接合が形成されるときに、下部接合は溶融及び固化工程を受けない。例えば、下部デバイスの場合、半田３６，３８は（例えば、約２８０℃の融点を有する）Ａｕ－Ｓｎ共融混合物半田からなり、一方、上部デバイスの場合、半田３６’，３８’は（例えば、約２１５℃の融点を有する）Ｓｎ－Ａｇ共融混合物半田からなる。別法として、下部デバイス用の第１の半田材料３６，３８は（例えば、約１８３℃の融点を有する）Ｓｎ－Ｐｂ共融混合物半田からなり、一方、上部デバイス用の第２の半田材料３６’，３８’は（例えば、約１３９℃の融点を有する）Ｂｉ－Ｓｎ共融混合物半田からなることもできる。また、融点序列を有する異なる半田を用いて、デバイスの多層垂直相互接続を形成することもできる。更に、半田とナノワイヤ又は回路パッド表面との間の界面接合力を高めるために、半田材料は場合により１種類以上のカーバイド生成元素を含有することもできる。

【００２６】垂直相互接続の形成に使用されるナノワイヤの寸法は微小であることが好ましい。各ナノワイヤの直径は一般的に、約２００ｎｍ未満であり、好ましくは５０ｎｍ未満であり、更に一層好ましくは１０ｎｍ未満である。各接続の高さ又は各ナノワイヤの長さは一般的に、約１０～１０００ｎｍの範囲内である。ナノワイヤの長さは望ましくは少なくとも１０ｎｍであり、好ましくは、憂くなくとも１００ｎｍであり、更に一層好ましくは少なくとも１０００ｎｍである。これにより、ナノワイヤは、高アスペクト比及び機械的コンプライアンシーを達成するのに十分に長くかつ薄い。しかし、ナノワイヤを過大に延ばすには束縛が存在する。ナノワイヤが長くなるほど、特にカーボンナノチューブの場合には、その全長にわたって電気特性を維持したり、垂直心合せを維持することが一層困難になる。また、長いナノワイヤは長いプロセスに至る。例えば、延長された長さを得るために、成長を長期間継続させなければならない。ナノワイヤの長さの上限は一般的に、１００μｍ未満であり、一層好ましくは２０μｍ未満であり、更に一層好ましくは２μｍ未満である。

【００２７】垂直に相互接続された構造物で使用されるナノワイヤは、直接導電性の他に、それ自体がデバイス特性を有することもできる。例えば、複合ナノワイヤは、ナノワイヤの長さに沿って存在する少なくとも一つのヘテロ接合を有することもできる。シリコン半導体ナノワイヤは金属性カーボンナノチューブの一端上に成長させることができ、またはこの逆も可能である。例えば、J.Hu et al., NATURE,Vol. 399 (1999), p. 48参照。金属－半導体ヘテロ接合を１個以上のナノワイヤに組み込み、整流ダイオードデバイスとして使用することができる。ｐ－ｎ接合又はトンネルデバイス構造物のようなその他のタイプのデバイスもナノワイヤ中に組み込むことができる。図６は、ナノワイヤ自体が金属性カーボンナノチューブ４ａ及び半導体ワイヤ４ｂの複合体か

らなる相互接続デバイスの模式的断面図である。下部回路基板１０はその表面に接点パッド１２ａ，１２ｂを有し、そしてナノワイヤはカーボンナノチューブ４ａからなるその部分で接点パッドと接合されている。上部回路基板１０'はその表面に接点パッド１２ａ'，１２ｂ'を有し、そして半導体ワイヤからなるナノワイヤ４ｂの上部部分はこれらの上部接点パッド１２ａ'，１２ｂ'と接合されている。これらの複合ナノワイヤは、溶解性基板上に整合並列形式で成長され、前記のように、その長さを等長化させ、そして、前記のように、この複合ナノワイヤを基板１０，１０'に半田接合させることができる。アレー構造をこのようなデバイスの高密度アセンブリーに使用することができる。

【００２８】例えば、ナノワイヤの初期成長のために溶解性基板を使用する代わりに、非溶解性基板又はその後の加工中の溶解処理に依拠しない溶解性基板を使用することができる。基板は一対の端部におけるナノワイヤから機械的に引き去り、分離させると同時に、他方の端部を例えば、半田接合により所望の回路パッドに強力に接合させておくことができる。この別法を使用する場合、基板－ナノワイヤ界面における接合力は、ナノワイヤ－パッド界面における接合力よりも大幅に低くなければならない。例えば、石英基板上に成長されたカーボンナノチューブは比較的低い接合力を有し、弱い機械力を使用することにより基板から容易に分離させることができる。

【００２９】

【発明の効果】以上説明したように、本発明によれば、便利な垂直相互接続に好適な自立性ユニットとして形成することができる概ね等しい長さのナノワイヤ及びこのようなナノワイヤを用いて垂直に相互接続された回路デバイスを得ることができる。

【図面の簡単な説明】

【図１】基板上に成長されたナノワイヤの様々な形状を示す模式図であり、（Ａ）はランダムな方向に成長したナノワイヤを示し、（Ｂ）は縺れた状態で成長したナノワイヤを示し、（Ｃ）は垂直方向に平行に成長した不均一な長さを有するナノワイヤを示し、（Ｄ）は等長化されたナノワイヤを示す。

【図２】垂直の相互接続されるデバイスを製造するのに＊有用な溶解性基板上に成長されたナノワイヤを示す模式図である。

【図３】ナノワイヤを概ね同じ長さに等長化させる方法の一例を示す模式図であり、（Ａ）は犠牲層を堆積させるステップを示し、（Ｂ）は犠牲層を堆積させた状態を示し、（Ｃ）は等長化させた状態を示し、（Ｄ）は犠牲層を除去した状態を示す。

【図４】ナノワイヤに金属被膜を被着させた様々な形状を示す模式図であり。（Ａ）ナノワイヤの片側に金属被膜を照準線蒸着させた状態を示し、（Ｂ）はナノワイヤの先端部に金属被膜を被着させた状態を示し、（Ｃ）はナノワイヤの全面に金属被膜を被着させた状態を示す。

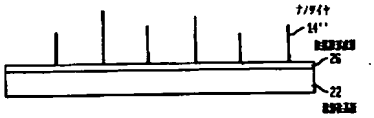
【図５】ナノワイヤを基板に接合させ、垂直相互接続を形成する方法の一例を示す模式図であり、（Ａ）は逆さま状態のナノワイヤを接点パッドに対面させた状態を示し、（Ｂ）はナノワイヤを接点パッドに接合させた状態を示し、（Ｃ）は基板を除去した状態を示し、（Ｄ）は上向きのナノワイヤに対して接点パッドを対面させた状態を示し、（Ｅ）は接点パッド同士をナノワイヤで垂直に相互接続させた状態を示す。

【図６】複合ナノワイヤを用いて垂直に相互接続されたデバイスを示す模式図である。

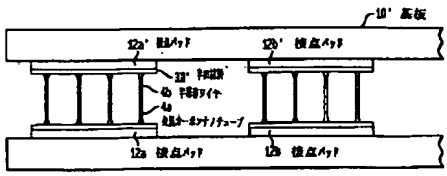
【符号の説明】

４ａ　金属カーボンナノチューブ
４ｂ　半導体ワイヤ
１０，１０'　基板
１１　基板表面
１２，１２ａ，１２ｂ，１２ａ'，１２ｂ'　接点パッド
１４，１４'，１４"　ナノワイヤ
１６ａ～１６ｇ　上部部分
２２　溶解性基板
２３　電源
２４　アノード
２５　電解質浴
２６　触媒核形成層
３０　犠牲層
３４　余分な長さ部分
３６，３６'　金属被膜（半田材料）
３８，３８'　半田材料

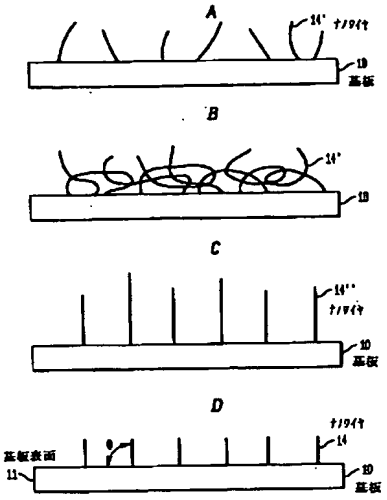
【図２】



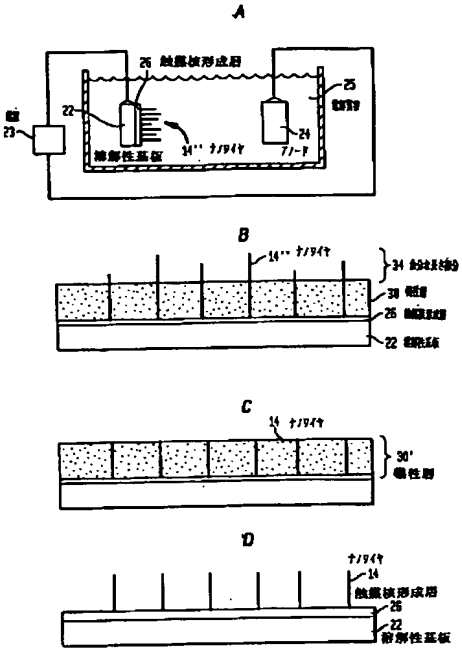
【図６】



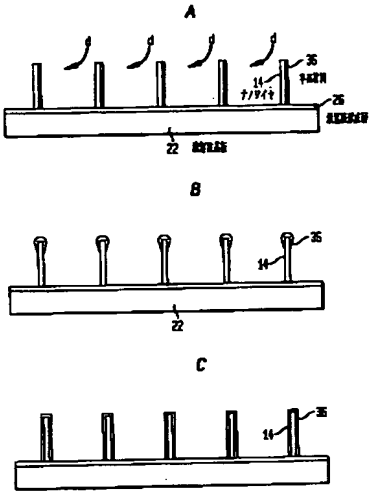
【図１】



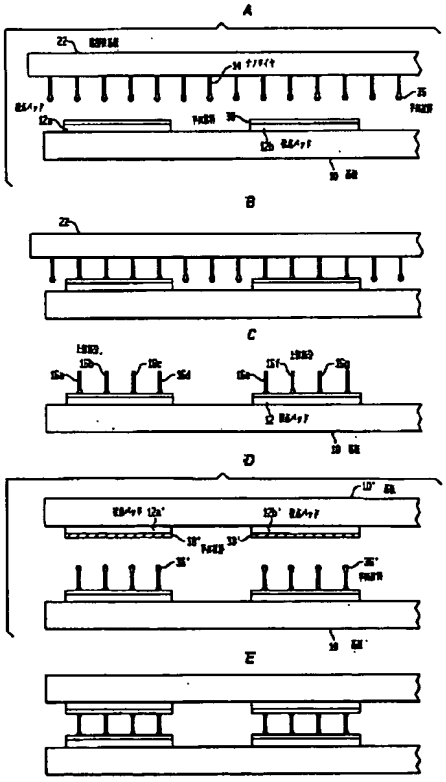
【図３】



【図４】



【図５】



フロントページの続き

(51)Int.Cl.[7]	識別記号	FI	ﾃｰﾏｺｰﾄﾞ(参考)
// Ｃ０１Ｂ　31/02	１０１	Ｃ２３Ｃ　16/26	
Ｃ２３Ｃ　16/26		Ｈ０１Ｌ　23/52	Ｃ

(71)出願人　596077259
600 Mountain Avenue, Murray Hill, New Jersey 07974－0636U. S. A.
(72)発明者　ウォルター　エル　ブラウン
アメリカ合衆国、07922　ニュージャージー、バークレー　ハイツ、ケンブリッジ　ドライブ　138
(72)発明者　スンゴ　ジン
アメリカ合衆国、07946　ニュージャージー、ミリントン、スカイライン　ドライブ　145
(72)発明者　ウェイ　ズ
アメリカ合衆国、07059　ニュージャージー、ウォーレン、シューマン　テラス　4

Ｆターム(参考)　4G046 CA02 CB01 CC06 CC08
4K030 AA09 BA27 BB00 DA02 DA08 JA01
5E344 AA01 AA22 BB02 BB06 CD13 CD14 DD02 DD05 EE11 EE21

【外国語明細書】

1. Title of Invention

Article Comprising Vertically Nano-InterConnected Circuit Devices And Method For Making The Same

2. Claims

1. An article having a circuit device comprising at least two circuit layers and a plurality of substantially equi-length nanowires disposed between and electrically interconnecting the at least two circuit layers.

2. The article of claim 1 in which each one of the plurality of nanowires has a diameter of less than 500 nm.

3. The article of claim 1 in which each one of the plurality of nanowires is substantially vertically aligned.

An article having a circuit device comprising at least two circuit layers and a plurality of substantially parallel and equi-length nanowires perpendicularly disposed and electrically interconnecting the at least two circuit layers, wherein each one of the plurality of nanowires has a diameter of less than 500 nm and is bonded to at least one of the two circuit layers by metallic solder bonding.

5. The article of claim 4 in which the plurality of nanowires exhibit mechanical compliancy for avoiding reliability problems associated with external stresses.

6. The article of claim 4 in which the plurality of nanowires are selected from carbon nanotubes, semiconductor nanowires, and nanowires fabricated with at least one of metals, alloys, oxides, carbides, nitrides, borides, or mixed ceramics.

7. The article of claim 4 in which the length of any one of the nanowires deviates from the average length of all the plurality of nanowires by less than twenty percent.

8. The article of claim 4 in which at least one of the plurality of nanowires comprises a composite nanowire having a heterojunction present along the length thereof.

9. A method of making a circuit device comprising:

providing a substrate;

growing a plurality of nanowires on the substrate so that each one of the plurality of nanowires has a first exposed end and a second end attached to the substrate;

equalizing the length of the nanowires so that each one of the plurality of nanowires is substantially equal in length;

bonding the first exposed ends of the plurality of nanowires to a first circuit layer; and

removing the substrate to provide a circuit device having the plurality of nanowires bonded to the first circuit layer with the second ends of the plurality of nanowires exposed.

10. The method of claim 9, wherein the step of removing the substrate comprises mechanically detaching the second ends of the plurality of nanowires from the substrate.

11. The method of claim 9 wherein the substrate comprises a dissolvable substrate and the step of removing the substrate comprises chemically dissolving the substrate.

12. The method of claim 9 further comprising the steps of providing a second circuit layer, coating the second exposed ends of the plurality of nanowires with a second soldering material, and bonding the second exposed ends to the second circuit layer to provide a vertically-interconnected circuit device.

13. The method of claim 9, in which the step of growing the plurality of nanowires comprises depositing a catalytic nucleation layer on the dissolvable substrate and decomposing a gas adjacent the catalytic nucleation layer.

14. The method of claim 13 in which the gas comprises a hydrocarbon-containing gas such that carbon nanotubes are grown on the dissolvable substrate.

15. The method of claim 9 further comprising the step of coating at least one of the first and second exposed ends of the plurality of nanowires with a soldering material.

16. The method of claim 15 in which the soldering material is applied to at least one of the first and the second exposed ends of the plurality of nanowires by a deposition process during which the dissolvable substrate is rotated to promote a uniform application of the soldering material on the plurality of nanowires.

17. The method of claim 15 in which the first and second circuit layers each has a plurality of contact pads thereon, a layer of soldering material is applied to each of the contact pads on the first and second circuit layer, and the first and second ends of the plurality of nanowires are bonded onto the contact pads.

18. The method of claim 17, in which the first soldering material used to bond the first exposed ends to the first circuit layer has a first soldering temperature and the second soldering material used to bond the second exposed ends to the second circuit layer has a second soldering temperature, in which the second soldering temperature is lower than the first soldering temperature.

19. The method of claim 9, in which the step of equalizing the length of the nanowires comprises:

partially embedding the plurality of nanowires attached to the dissolvable substrate in a layer of sacrificial material of substantially uniform thickness whereby an extra length of nanowires protrudes from the sacrificial material;

removing the extra length of nanowires; and

removing the sacrificial material.

20. The method of claim 19, further comprising a conductive underlayer interposed between the dissolvable substrate and the catalytic nucleation layer for use in enhancing adherence of the layer of sacrificial material to the dissolvable substrate.

21. The method of claim 19, in which the sacrificial material is deposited by electroplating.

22. The method of claim 19, in which the thickness of the layer of sacrificial material is in the range of about 1 to 100 micrometers.

23. An article according to claim 1 wherein the plurality of nanowires have an average diameter of less than 200 nm and contain at least one of a semiconductor p-n junction and tunnel junction.

24. An article comprising an array of vertically interconnected nanowire rectifying diode devices according to claim 1.

3. Detailed Description of Invention

Related Applications

This application is related to U.S. patent application Serial No. _____, titled "*Tactile Sensor Comprising Nanowires and Method for Making the Same*," filed Sept. 24, 1999, by inventor Jin herein, and U.S. patent application Serial No. _____, titled "*In-Situ Nano-interconnected Circuit Devices and Method for Making the Same.*" filed concomitantly herewith, by inventors Brown, Jin and Zhu herein.

Field Of The Invention

This invention relates to structures for making nano-interconnected or nano-packaged circuits and methods of making same, and more particularly, to vertical electrical connection of circuits using conductive nanowires.

Background Of The Invention

Nano-scale wires such as carbon nanotubes with a very small size scale, on the order of 1-100 nanometers in diameter and 0.1-100 μm in length, have received considerable attention in recent years. *See* Liu *et al.*, SCIENCE, Vol. 280, p. 1253 (1998); Ren *et al.*, SCIENCE, Vol. 282, p. 1105 (1998); Li *et al.*, SCIENCE, Vol. 274, p. 1701 (1996); Frank *et al.*, SCIENCE, Vol. 280, p. 1744 (1998); J. Tans *et al.*, NATURE, Vol. 36, p. 474 (1997); Fan *et al.*, SCIENCE, Vol. 283, p. 512 (1999); Collins *et al.*, SCIENCE, Vol. 278, p. 100 (1997); Kong *et al.*, NATURE, Vol. 395, p. 878 (1998); and Ebbesen *et al.*, NATURE, Vol. 382, p. 54 (1996).

Carbon nanotubes exhibit unique atomic arrangements, nano-scale structures and interesting physical properties such as one-dimensional electrical behavior, quantum conductance, and ballistic transport characteristics. The ballistic transport in carbon

nanotubes, as reported by Frank *et al*, allows the passage of huge electrical currents in electronic circuits, with the magnitude of current density comparable to or better than those in some superconductors. Carbon nanotubes are one of the smallest dimensioned nanowire materials with generally high aspect ratio and small diameter of ~ 1 nm in the case of single-wall nanotubes and less than ~50 nm in the case of multi-wall nanotubes. *See* Rinzler *et al*, APPLIED PHYSICS, Vol. A67, p. 29 (1998); Kiang *et al*, J. PHYSICAL CHEM., Vol. 98, p. 6612 (1994), and Kiang *et al*, PHYSICAL REVIEW LETTERS, Vol. 81, p. 1869 (1998).

High-quality single-walled carbon nanotubes are typically grown as randomly oriented, needle-like or spaghetti-like, tangled nanotubes by laser ablation or arc techniques (a chemical purification process is usually needed for arc-generated carbon nanotubes to remove non-nanotube materials such as graphitic or amorphous phase, catalyst metals, etc). Chemical vapor deposition (CVD) methods such as used by Ren *et al*., Fan *et al*., and Li *et al* tend to produce multiwall nanotubes attached to a substrate, often with a semi-aligned or an aligned, parallel growth perpendicular to the substrate. As described in these articles, catalytic decomposition of hydrocarbon-containing precursors such as ethylene, methane, or benzene produces carbon nanotubes when the reaction parameters such as temperature, time, precursor concentration, flow rate, are optimized. Nucleation layers such as a thin coating of Ni, Co, Fe, etc. are often intentionally added to the substrate surface to nucleate a multiplicity of isolated nanotubes. Carbon nanotubes can also be nucleated and grown on a substrate without using such a metal nucleating layer, e.g., by using a hydrocarbon-containing precursor mixed with a chemical component (such as ferrocene) which contains one or more of these catalytic metal atoms. During the chemical vapor decomposition, these metal atoms serve to nucleate the nanotubes on the substrate surface. *See* Cheng *et al.*, CHEM. PHYSICS LETTERS, Vol. 289, p. 602 (1998).

The modern trend in electronic circuit design, interconnection and packaging is toward use of finer features, such that submicron feature sizes have been reached in recent years. To produce desired, ultra-high density electronic packaging, a small width of the circuit lines is important, as well as a three-dimensional, multi-layer configuration

with vertically integrated circuit layers. However, nanowires grown with presently-available methods are not suitable for such purposes. The as-grown single-wall nanotubes (SWNT) such as commonly synthesized by laser ablation or arc method, have a spaghetti-like configuration and often are tangled with each other. The multi-wall nanotubes (MWNT), such as commonly made by chemical vapor deposition, are easier to prepare in an aligned and parallel configuration. However, these as-grown nanotubes such as reported by Ren *et al.* and Li, *et al.* differ in height or length. For reliable circuit interconnections without electrical shorts or opens, it is desirable to prepare nanowires having equal and specific predetermined lengths. Further, it would be advantageous to provide the nanowires as free-standing wires so that they may be manipulated, e.g., for transfer, placement and bonding for circuit interconnections at ambient or relatively low temperatures, e.g., below 300°C. Selective CVD growth of nanowires such as carbon nanotubes directly on desired circuit pads may be possible using selective area patterning of a catalyst layer; however, often it is undesirable to expose the delicate semiconductor circuits and components to the high temperatures (e.g., 600 -1000°C) and chemical environments involved with CVD deposition of nanotubes. The invention discloses substantially equal length nanowires that may be fabricated as free-standing units suitable for convenient vertical interconnections and vertically interconnect circuit devices using such nanowires.

Summary Of The Invention

The invention comprises a vertically-interconnected circuit device having at least two circuit layers and a plurality of substantially equi-length nanowires disposed therebetween. The nanowires may comprise composites, e.g., having a heterojunction present along the length thereof, to enable a number of device applications. Also disclosed is a method for making the circuit device comprising growing a plurality of nanowires on a removable substrate, equalizing the length of the nanowires (e.g., so that each one of the plurality of nanowires is substantially equal in length), transferring and bonding exposed ends of the plurality of nanowires to a first circuit layer; and removing the substrate. The nanowires attached to the first circuit layer can be further bonded to a second circuit layer to provide the vertically-interconnected circuit device.

Brief Description Of The Drawings

For a better understanding of the invention, an exemplary embodiment is described below, considered together with the accompanying drawings, in which:

FIGS. 1A-1D schematically illustrate various configurations of nanowires grown on a substrate;

FIG. 2 schematically illustrates nanowires grown on a dissolvable substrate useful in making the vertically interconnected devices;

FIGS. 3A-3D schematically illustrate an exemplary process for equalizing nanowires to substantially the same length; and

FIGS. 4A-4C show various configurations for the deposition of metallic coatings on nanowires;

FIGS. 5A-5E schematically illustrate an exemplary process for attaching nanowires to a substrate and making vertical interconnections; and

FIG. 6 schematically shows a vertically interconnected device using composite nanowires.

It is to be understood that these drawings are for the purposes of illustrating the concepts of the invention and are not to scale. Like reference numerals are used in the figures to refer to like features.

Detailed Description Of The Invention

This application discloses methods for preparing electrically-conducting nanowires such as carbon nanotubes that are useful as nano-scale, vertically connecting wires between circuit device layers and for in-plane connecting wires between adjacent electrical contact pads. For circuit interconnections, such as between two circuit layers or mating devices, the use of many, sub-divided parallel conductive paths can be achieved with aligned nanowires. The nanowires provide elastic compliance and

flexibility of the interconnection medium which are advantageous in avoiding short and long-term reliability problems, e.g., caused by undesirable stresses. Common sources of stresses exerted on the interconnection medium include local temperature gradients, stresses arising from mismatches of the thermal expansion coefficients between different materials used in the devices, and electromigration-induced stresses, and mechanical and thermal stresses introduced during device assembly, handling, testing, or shipping. The invention avoids or minimizes the reliability problems caused by such stresses including fatigue, creep, or deformation failures of the interconnection medium or circuit components. When small-diameter nanowires are utilized, this invention is useful for achieving high- or ultra-high density circuit interconnections.

Referring to the figures, FIGS. 1A-1D schematically illustrate various configurations of nanowires grown on a substrate 10. The nanowires may comprise carbon nanotubes; semiconductor nanowires fabricated, for example, with Si, Ge, or GaAs; or nanowires fabricated with any other conductive or nonconductive materials known in the field, such as metals, alloys, oxides, carbides, nitrides, borides, or mixed ceramics. Methods for fabricating the nanowires may comprise laser ablation, arc discharge, or chemical vapor deposition of a precursor gas or mixture of precursor gases. Small diameter nanowires may be nucleated and grown upward from the substrate by catalytic decomposition of a gas phase. In this case, a catalytic film may be deposited on the substrate and fine-scale, local nucleation of this film may be initiated with catalytic decomposition in a gas phase. For example, a glass circuit substrate may be provided, a catalytic film comprising a transition metal may be deposited on the glass substrate, and then carbon nanotubes may be fabricated by decomposing C_2H_4 on the film surface. The catalytic film is also referred to herein as the catalytic nucleation film; it may be comprised of Ni, Co, or Fe, or other materials known in the field.

In the absence of alignment processing, the nanowires tend to grow as randomly-oriented or tangled nanowires 14', as shown in FIGS. 1A and 1B, respectively. A tangled morphology of nanowires 14' (FIG. 1B), also may be obtained with use of laser ablation. However, advantageously for the use in vertical interconnections, the nanowires are substantially vertically aligned. The nanowires may be aligned as they are

fabricated, e.g., by using an applied electrical field, gas concentration gradient, or temperature gradient. Also, the nanowires may be aligned as grown by physical techniques using recessed vertical cavities in the substrate or by crowding, e.g., simultaneously fabricating a "dense forest" of nanowires (e.g., a high concentration per unit area). A porous ceramic or silicon layer may be used in combination with a catalytic nucleation film to enhance aligned growth of the nanowires. The aligned nanowires may be of a non-uniform length 14'', as in FIG. 1C, or of a uniform length 14, as in FIG. 1D. The embodiment shown in FIG. 1D is preferred, that is, where the nanowires are substantially aligned and substantially equal in length. The length of each of the nanowires preferably deviates from the average nanowire length by less than 20% and more preferably by less than 10%.

The nanowires 14 advantageously are vertically aligned relative to the substrate and disposed substantially in parallel. Full vertical alignment of the nanowires (e.g., where in FIG. 1D angle ϕ between the surface 11 of the substrate and the length of the nanowire is 90°) is not necessary. However, preferably the deviation from complete vertical alignment is insubstantial, that is, it is less than about 25 degrees and preferably less than 15 degrees from full (90°) alignment.

For ease of use in making vertical interconnections, the nanowires may be grown on a separate substrate that is dissolvable. For example, FIG. 2 shows unequal length vertically aligned nanowires 14" on a dissolvable substrate 22, grown with use of a catalytic nucleation layer 26. The dissolvable substrate aids in transferring the nanowires in making circuit interconnections, as explained below. The dissolvable substrate layer may be dissolvable in water, acid, base, or solvents. For example, sodium chloride crystal may be used to fabricate a water-soluble substrate. To fabricate an acid-dissolvable substrate, metals such as Cu, Ni, Co, Mo, Fe, V, Au, Ag, or their alloys may be used. To fabricate a base-dissolvable substrate, metals such as Al may be used. The substrate should be chosen so that the temperature of nanowire growth, e.g., by CVD processing, is below the melting point of the substrate material used. Alternatively, dissolvable polymer materials may be used to fabricate the separate substrate layer, such

as polyvinyl alcohol, polyvinyl acetate, polyacrylamide, acrylonitrile-butadiene-styrene, or volatile (evaporable) materials such as polymethylmethacrylate (PMMA). When polymers are used, the temperature used in processing the nanowires should be sufficiently low to avoid damaging the polymer, such as through decomposition, change in physical shape, or change in chemical properties. A combination of materials also may be used to fabricate the dissolvable substrate layer. The dissolvable substrate may be coated with the catalytic nucleation film 26 (e.g., Ni, Fe, or Co) to grow the nanowires. After the nanowires are grown, the dissolvable layer can be removed. The catalytic nucleation film may be deposited on the dissolvable layer as a continuous layer or in a spotted or patterned manner, e.g., by sputtering, evaporation, or electrochemical deposition.

Nanowires may be first grown of unequal length, as shown in FIGS. 1C and 2, and then an equalization process applied to achieve substantially equal length nanowires, as shown in FIG. 1D. As mentioned, substantially equal-length nanowires are preferred. *See*, for example, US patent application Serial No. 09/354,928, "*Nanoscale Conductive Connectors and Method for Making Same*," filed July 15, 1999, by Choi and Jin, inventors herein, assigned to the present assignee and incorporated herein by reference. An example of an equalization process is schematically illustrated with reference to FIGS. 3A-3D. The equalization process of this example comprises essentially three steps, i.e. (1) embedding unequal length nanowires in a dissolvable sacrificial layer 30 having a substantially uniform thickness (FIGS. 3A-3B); (2) removing an extra length 34 of nanowires protruding from the sacrificial layer (FIG. 3C); and (3) removing the sacrificial layer (FIG. 3D). Of course, it is understood that other equalization processes in the field may be used, such as laser cutting and hot blade cutting. *See, e.g.*, U.S. Patent application Serial No. 09/236,933 filed on January 25,1999 by Jin, Zhu *et al*, two inventors herein, assigned to the present assignee and incorporated herein by reference.

In the exemplary process of FIGS. 3A-3D, the first step involves depositing a sacrificial layer of substantially uniform thickness. FIG. 3A shows an electroplating apparatus and process for depositing the sacrificial layer 30 on a substrate 22 having unequal length nanowires 14." In this example, a copper (Cu) dissolvable substrate

layer 22 is provided, on which is deposited a catalytic nucleation layer 26 of nickel (Ni) having a thickness of about 1-100 nm. Of course, other materials as aforementioned may be used for the dissolvable substrate layer 22 or nucleation layer 26. The nucleation layer 26 is shown in the figures as a continuous layer. However, the nucleation layer (e.g., even when deposited as a continuous layer) may break up into segments or islands when heated, e.g., during chemical vapor deposition and nanowire growth. Such segmentation of the nucleation layer leaves the surface of the dissolvable substrate between nanowires depleted, without an overlying conducting metal film. Depending on the materials comprising the dissolvable substrate, it may be difficult to coat the substrate and segmented nucleation layer with a metallic sacrificial layer 30 (FIG. 3C, described below), such as, for example, where the dissolvable substrate is insulating (e.g., comprised of sodium chloride). Thus, a non-catalytic conductive underlayer (not shown) may first be deposited on the dissolvable substrate before the nucleation layer is deposited. In other words, in FIG. 2, an underlayer may be interposed between the dissolvable substrate 22 and the nucleation layer 26. This underlayer may be comprised of Mo or other non-catalytic conductive materials known in the field.

The Cu substrate layer 22 functions as a cathode in this process; it is positioned in a bath of electrolytic material 25 adjacent an anode 24 (e.g., of nickel) and coupled with the anode through power supply 23. The electrolyte 25 contains ions of the metal to be deposited, e.g., Ni from a solution containing $NiSO_4$ or Cu from a solution of $CuSO_4$. Preferably, the electrolyte bath 25 contains the same type of ions as those of the nucleation layer 26 or conductive underlayer. In this way, electrodeposition of the sacrificial layer 30 will occur on the surface of the nucleation layer 26 instead of on the nanowires 14'', such as carbon or silicon nanowires, due to chemical affinity, e.g., the sacrificial layer 30 has the same metallic characteristics as the nucleation layer and substantially different characteristics from the nanowires. The sacrificial layer is deposited to a thickness that is substantially the same as the desired length of the nanowires. This parameter (nanowire length) will depend on the desired application for the sensor, but typically it will be in the range of 1 to 100 micrometers, as mentioned above. The thickness of the sacrificial layer may be controlled with processing variables,

such as time, temperature, electrolyte concentration, current density, and so forth. Of course, FIG. 3A reflects one exemplary method for depositing the sacrificial layer. The sacrificial layer can be deposited by other methods, such as electroless plating, chemical vapor deposition, or physical vapor deposition, including sputtering, evaporation, laser ablation, or ion beam deposition.

FIG. 3B shows the structure obtained via the electrodeposition process of FIG. 3A comprising the dissolvable substrate layer 22; the nucleation layer 26; and the unequal length nanowires 14'' embedded in the sacrificial layer 30 of substantially uniform thickness. The nanowires 14'' each have an exposed extra-length portion 34 protruding beyond the sacrificial layer 30. The sacrificial layer 30 temporarily protects the buried nanowires while the extra-length portion 34 is removed. The sacrificial layer desirably is comprised of an easily-removable material, e.g., one that is removable by dissolving it in water or a solvent, by chemical or electrochemical etching, or by vaporizing through heating. Examples of suitable water-soluble or solvent-soluble materials include salts such as sodium chloride, silver chloride, potassium nitrate, copper sulfate, and indium chloride, or organic materials such as sugar and glucose. Examples of suitable chemically-etchable materials include metals and alloys such as Cu, Ni, Fe, Co, Mo, V, Al, Zn, In, Ag, Cu-Ni, and Ni-Fe. Sacrificial layers formed of these materials may be dissolved away in an acid such as hydrochloric acid, aqua regia, or nitric acid, or in a base solution such as sodium hydroxide or ammonia. Suitable vaporizable materials include those that exhibit high vapor pressure such as Zn, or which can be decomposed or burned away by heat treatment in a suitable oxidizing, reducing, or neutral gas atmosphere, such as organic acids.

A next step of the equalization process involves removing the exposed portions 34 of the nanowires to obtain the equi-length nanowires 14 embedded in the sacrificial layer 30', as shown in FIG. 3C. Polishing or etching the exposed portions 34, e.g., by chemical or mechanical methods may perform this removal. Heating also may be used, which is preferred when carbon nanowires are used. For example, the extra-length portion 34 may be removed by heating the structure in an oxidizing atmosphere, e.g., at temperatures in the range of 200 to 1000°C. A full or partial oxygen or ozone

atmosphere may be used. Alternatively, mechanical polishing may be used to remove the extra length of the nanowires. In the next step, the sacrificial layer 30' having equal length nanowires (FIG. 3C) is removed, e.g., by being dissolved away. The structure of FIG. 3D is thus achieved, having the substrate 22, nucleation layer 26, and substantially equal-length nanowires 14.

In removing the sacrificial layer 30', the nucleation layer 26 should remain on the dissolvable substrate 22, because otherwise, the nanowires may detach from the substrate 22. If the sacrificial layer comprises a non-metallic layer such as sodium chloride, copper sulfate, or polyvinyl alcohol, the sacrificial layer may be removed with the nucleation layer remaining in tact. However, if the sacrificial layer comprises a metal layer, removal of the sacrificial layer, such as by acid etch, may result in removal of the nucleation layer, such that the nanowires are detached from the substrate. To address this situation, the sacrificial layer may be partially etched (e.g., to one-half or one-third its original thickness), to expose a sufficient length of the nanowires for connecting the exposed ends of the nanowires to a circuit device. In this case, the remaining sacrificial layer may be removed later, e.g., when the dissolvable substrate and nucleation layer are removed. Advantageously, the dissolvable substrate is coated with a temporary protective layer (not shown) to protect it (e.g., from deformation, from being dissolved, etc.) during intermediate processing steps. The protective layer may be applied to the back and/or sides of the dissolvable substrate. It may comprise a lacquer-type material that is easily removed with solvents (e.g., alcohol or acetone) but stable in aqueous solutions. The materials comprising the dissolvable substrate 22, nucleation layer 26 and sacrificial layer 30 may be selected so that they have sufficient differential etching or removal rates to avoid dissolving the nucleation layer with removal of the sacrificial layer and/or to avoid damage to the dissolvable substrate during processing.

The equi-length parallel nanowires held by the dissolvable substrate (e.g., as in FIG. 3D) are useful for a variety of device applications, including vertical nano-scale circuit interconnections and tactile sensor devices, as described in U.S. application Serial No. _____, filed Sept. 24, 1999 by inventor Jin, which is incorporated herein by reference. Advantageously for certain applications, at least a portion of the nanowires

may be coated with a thin film or coating 36 of an electrically conductive and preferably bondable (solderable) metal or alloy (e.g., FIGS. 4A-4C). Optionally an adhesion-promoting layer (not shown) may be deposited between the coating 36 and the nanowire 14. Metallizing the nanowires may be helpful to ensure that there is electrical conduction along the length of the nanowires. The coating 36 may be applied to at least a portion of the nanowires and comprise a thin film of electrically conductive and preferably bondable (solderable) metal or alloy, for example, a solderable metal film such as Au, Ag, Pd, Rh, Ni, Cu, In, Sn, or a solder alloy film such as Au-Sn, Sn-Ag, Pb-Sn, Bi-Sn, In-Sn, or In-Ag. In the case of carbon nanotubes or nitride-type nanowires, the adhesion-promoting interface layer between the coating and nanowire may comprise a carbide- or nitride-forming element (e.g., Ti, Mo, Nb, V, Fe, W, Zr). The solderable layer as well as the adhesion-promoting layer can be added onto the nanowire surface by a number of processing approaches such as physical vapor deposition (sputtering, evaporation, ion-beam deposition), chemical vapor deposition, electroless or electrolytic deposition, or a combination of deposition techniques. Alternatively, the adhesion-promoting element may be pre-incorporated into the solder or solderable coating layer itself as an alloying element. To further promote the adhesion between the nanowire surface and the deposited adhesion-promoting layer, or between the adhesion-promoting layer and the solderable layer, an optional adhesion-enhancing heat treatment may be added, e.g., at about 100-900°C for 0.1 to 100 hours, in an inert or vacuum atmosphere.

FIGS. 4A-4C illustrate the metallic coating 36 as applied with various techniques. FIG. 4A, for example, shows a line-of-sight deposition of metal atoms via physical vapor deposition. The deposition is performed along a lateral direction, e.g., following arrows "d", such that the metal is concentrated on one side of the nanowires. A more uniform deposition over the surface of the nanowires can be obtained by a modified process, e.g., by rotating the substrate during the deposition. An electrochemical method for depositing the metal (for example, electrolytic or electroless deposition) can produce a preferentially localized deposition as shown in FIG. 4B. This preferential deposition can occur due to a generally higher electrolyte concentration or higher (concentrated) current density near the tips of the nanowires. A non-uniform profile also may be

obtained with CVD processing, with the uniformity of the coating dependent on various processing parameters, such as the speed at which the metal ions travel, the gas atom transfer to the deposition site, and the speed at which the coating is deposited. Slower and more controlled deposition processing can result in metallic coatings 36 of substantially uniform thickness along the length of the nanowires, as shown in FIG. 4C. The desirable thickness of the metallic or solderable layer as well as the interface adhesion-promoting layer (if needed) is typically in the range of 0.5-50 nanometers, and preferably is in the range of 1-20 nanometers.

The metallic film coated on the nanowires may serve several important functions.

i) It provides solderability for attaching the nanowires to the circuit substrate. A solderable metal or solder alloy coating is desirably also added to the surface of the electrical contact pads onto which the nanowires are to be bonded.

ii) It may impart a uniform electrical conductivity especially to nonmetallic nanowires, e.g., to semiconducting carbon nanotubes, semiconductor nanowires such as Si or Ga-As, or insulating nanowires such as Al_2O_3, SiO_2, BN, or other insulating ceramic nanowires. In fabricating efficient and reliable vertical interconnections, a stable electrical continuity from one end of the nanowire bonded to a bottom circuit device, through the nanowire length, and to the other end of the nanowire bonded to an upper device or the upper circuit layer is important. Single-wall nanotubes can be metallic with the "armchair" configuration of carbon atoms or semiconducting to near insulating with the "zig-zag" type configuration or certain "chiral" configurations. *See* Dresselhous *et al.*, Science of Fullerines and Carbon Nanotubes, Chap. 19 (Academic Press, San Diego 1996), at pp. 758, 805-809. It is also known that the nanotube atomic arrangements and hence electrical properties may vary drastically along the length of a single carbon nanotube. *See* Collins et al., SCIENCE, Vol. 278, p. 100 (Oct. 3, 1997). Such a variation in electrical properties may adversely effect the efficient electron transport between nano-interconnected devices via the carbon nanotube interconnection medium. The metal surface coating on the nanowires as herein described addresses this problem and provides the desired electrical conductivity to the vertical nano-interconnection medium.

iii) The coating can also provide corrosion/oxidation resistance to the solderable coating (and also to the nanowires themselves if they are susceptible to corrosion/oxidation) upon exposure to ambient or processing atmospheres. Noble metal films such as Au, Ag, Pd, Rh, and so forth can be utilized either as the coating itself or as an added overcoating on top of the solderable metal coating 36 deposited on the nanowire. A thin overcoating of noble metal such as Au can be easily absorbed into the underlying molten solder, e.g. Au-Sn or Pb-Sn eutectic solder, during the soldering process and thus does not prevent the bonding.

FIGS. 5A through 5E schematically illustrate an exemplary process for attaching nanowires to a substrate and making vertical interconnections. As illustrated in FIG. 5A, the dissolvable substrate 22 having substantially equal length nanowires 14 coated with a metallic solderable coating is placed upside down. A circuit substrate 10 having contact pads 12a, 12b thereon is placed facing the nanowires. The material used for making the contact pads can be selected from a number of different conductive materials, for example, those commonly used in semiconductor circuit fabrication, e.g., Al, Cu, W, Ta, TiN, TaN, $CoSi_2$, with an optional use of additional surface conductive coating. The contact pads also preferably are coated with a solderable layer 38. The contact pads 12a, 12b, etc., typically are less than 25 microns square in area, preferably less than 1 micron square in area, and even more preferably less than 0.01 microns square in area.

In FIG. 5B, the nanowires are in physical contact with the contact pads, and the structure is heated to induce solder bonding of the nanowires onto the pads. If the nanowires are not sufficiently strong to support the dissolvable substrate (e.g., against the force of gravity), spacers having a desired thickness may be used to prevent collapse of, or damage to, the nanowires by the weight of the substrate. The spacers may comprise a pre-deposited patterned thin film on the circuit substrate 10. The distribution of the nanowires 14 on the dissolvable layer 22 can be patterned so that it will match the location of the contact pads. This can be accomplished, for example, by lithographically patterning the catalytic nucleation layer 26 (FIG. 2) for growth of the nanowires during CVD processing.

In FIG. 5C, the dissolvable substrate 22 and also, if present, the catalytic nucleation layer 26, have been removed so that the nanowires are bonded to the circuit substrate 10 with their top portions 16a, 16b, 16c, etc., exposed. The nanowires may be further coated with a soldering material, e.g., as described earlier in connection with FIGS. 4A through 4C, so that their top exposed portions are again coated with solder 36', as shown in FIG. 5D. A mating device is provided, comprising a circuit substrate 10' with contact pads 12a' 12b' (FIG. 5D), and a layer of solder material 38' may be placed on the contact pads 12a', 12b.' The mating substrate 10' is placed in contact with the exposed nanowires, e.g. by the circuit device being placed upside down. The structure is then heated so the components are soldered together to complete the vertical interconnection, as shown in FIG. 5E. Spacers or micro-positioning device holders (not shown) may be placed on either or both circuit substrates 10, 10', for use in vertically positioning the devices prior to solder bonding.

The solder material 36', 38', used for bonding the upper device 10' to the top portions 16a, 16b, 16c, of the nanowires may be the same material used in bonding the lower device 10 to the bottom portions of the nanowires (e.g., 36, 38). In that case, the lower solder bonds will undergo the melting and solidification process at least a second time. Alternatively, a first solder material is used to bond the lower device, and a second solder material having a lower soldering temperature is used to bond the upper device. In this way, the lower bonds will not undergo the melting and solidification process when the upper bonds are formed. For example, for the lower device, the solder 36, 38 may comprise a Au-Sn eutectic solder (e.g., having a melting point of about 280°C), while for the upper device, the solder 36', 38' may comprise a Sn-Ag eutectic solder (e.g., having a melting temperature of about 215°C). Alternatively, the first soldering material 36, 38 for the lower device may comprise a Pb-Sn eutectic solder (having a melting temperature of about 183°C), while the second soldering material 36', 38' for the upper device comprises a Bi-Sn eutectic solder (e.g., having a melting temperature of about 139°C). A multi-layer vertical interconnection of devices also may be carried out using different solders with a hierarchy of melting points. Additionally, the soldering materials optionally may contain one or more carbide forming elements to improve the interface

bonding between the solder and the nanowire or circuit pad surface.

The nanowires used in making the vertical interconnections preferably have small dimensions. The diameter of each nanowire is typically less than about 200 nm, preferably less than 50 nm, and even more preferably less than 10 nm. The height of each connection, or the length of each nanowire, is typically in the range of about 10 to 1000 nm. The length of the nanowires desirably is at least 10 nm, preferably at least 100 nm, and even more preferably at least 1000 nm so that they are sufficiently long and thin to achieve a high aspect ratio and mechanical compliancy. However, there are constraints to lengthening the nanowires too much. The longer the nanowires, the more difficult it is to maintain electrical properties over their length (particularly in the case of carbon nanotubes), or to maintain the vertical alignment. Also, a longer nanowire translates to a longer process, e.g., the growth must continue for a longer period of time to achieve the extended length. An upper limit for the nanowire length typically may be less than 100 micrometers, more preferably less than 20 micrometers, and even more preferably less than 2 micrometers.

The nanowires used for the vertically-interconnected structures can also possess device characteristics in themselves, i.e., besides straight-forward electrical conduction. For example, a composite nanowire may have at least one heterojunction present along the length of the nanowire. It is known that a silicon semiconductor nanowire can be grown onto the end of a metallic carbon nanotube, or vice versa. *See, e.g.*, J. Hu *et al.*, NATURE Vol. 399 (1999), at p. 48. The metal-semiconductor heterojunction can be integrated into one or more of the nanowires to serve as a rectifying diode device. Other types of devices such as p-n junctions or tunneling device structures also may be incorporated into the nanowires. FIG. 6 schematically illustrates an interconnected device where the nanowires themselves comprise composites of metallic carbon nanotubes 4a and semiconductor wires 4b. A lower circuit substrate 10 has contact pads thereon 12a, 12b, and the nanowires are bonded thereto at portions thereof comprising carbon nanotubes 4a. An upper circuit substrate 10' has contact pads thereon 12a', 12b', and the upper part of the nanowires 4b comprising semiconductor wires are bonded to these upper contact pads 12a', 12b.' These composite nanowires may be

grown in an aligned parallel fashion on a dissolvable substrate and their lengths equalized, as described above, and they may be solder bonded to the substrates 10, 10', also as described above. An array structure can be used for a high-density assembly of such devices.

It is understood that the embodiments described herein are merely exemplary and that a person skilled in the art may make many variations and modifications without departing from the spirit and scope of the invention. For example, instead of using a dissolvable substrate for the initial growth of nanowires, one could use a non-dissolvable substrate or a dissolvable substrate without resorting to the dissolution approach during subsequent processing. The substrate can be mechanically pulled away and separated from nanowires at one set of ends while the other ends are strongly bonded onto the desired circuit pad, e.g., by solder bonding. When this alternative approach is used, the bond-strength at the substrate-nanowire interface should be substantially lower than that at the nanowire-pad interface. For example, carbon nanotubes grown on a quartz substrate will have a relatively weak bond strength and can be easily separated from the substrate by use of a weak mechanical force. All such variations and modifications are intended to be included within the scope of the appended claims.

4. Brief Description of Drawings

Written above.

FIG. 1A

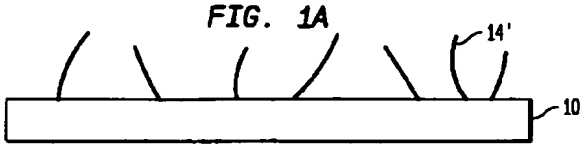


FIG. 1B

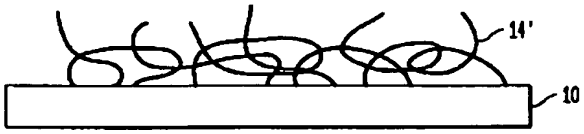


FIG. 1C

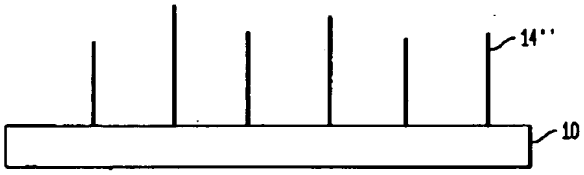


FIG. 1D

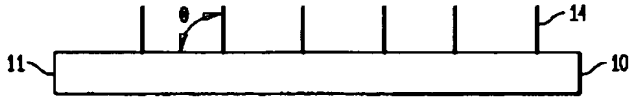


FIG. 2

FIG. 3A

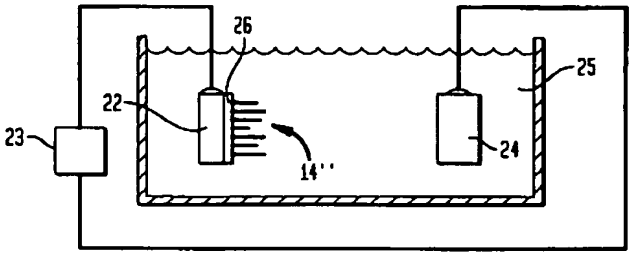


FIG. 3B

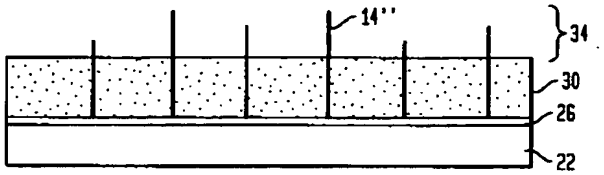


FIG. 3C

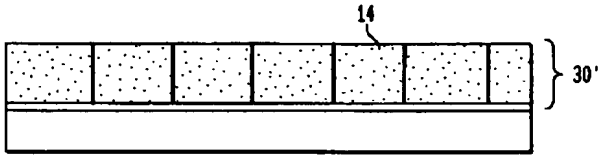


FIG. 3D

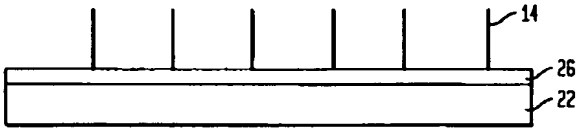


FIG. 4A

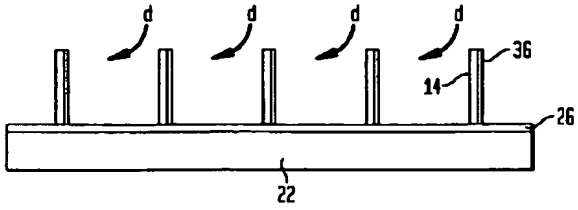


FIG. 4B

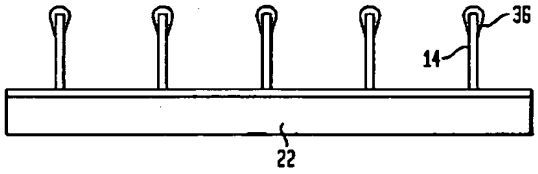


FIG. 4C

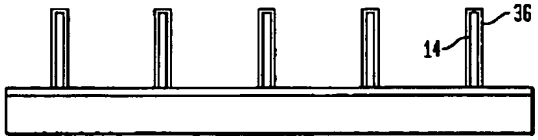


FIG. 5A

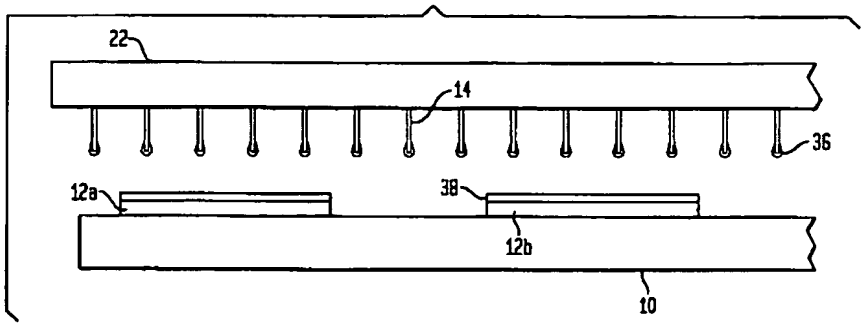


FIG. 5B

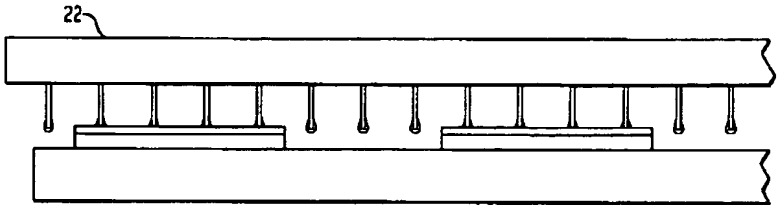
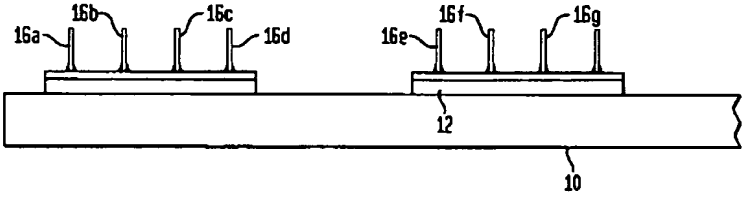


FIG. 5C



5/5

FIG. 5D

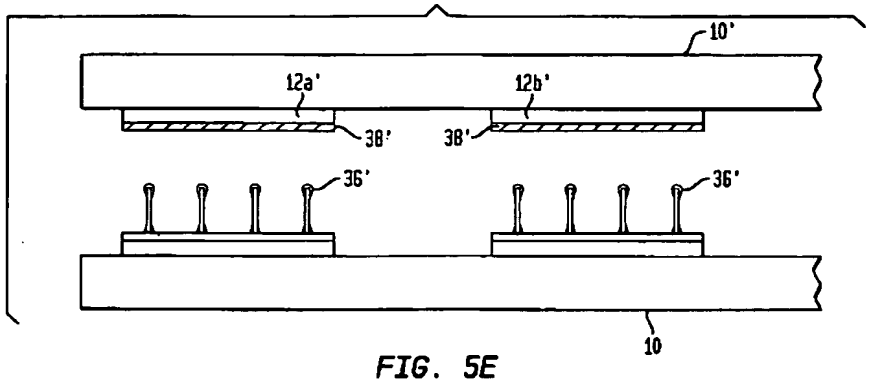


FIG. 5E

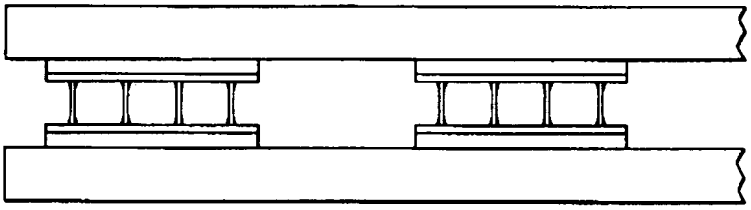
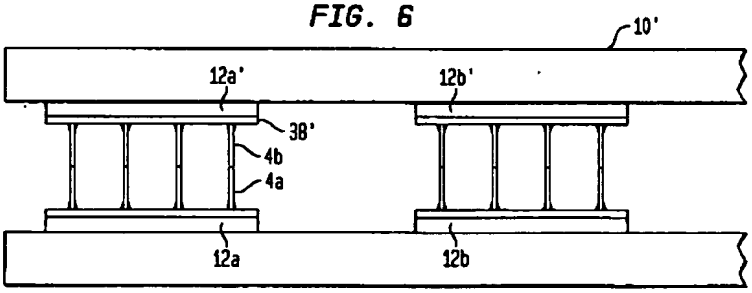


FIG. 6



1 Abstract

A circuit device is disclosed comprising at least two circuit layers or circuit devices vertically interconnected with a plurality of parallel and substantially equi-length nanowires disposed therebetween. The nanowires may comprise composites, e.g., having a heterojunction present along the length thereof, to provide for a variety of device applications. Also disclosed is a method for making the circuit device comprising growing a plurality of nanowires on a dissolvable or removable substrate, equalizing the length of the nanowires (e.g., so that each one of the plurality of nanowires is substantially equal in length), transferring and bonding exposed ends of the plurality of nanowires to a first circuit layer, and removing the dissolvable substrate. The nanowires attached to the first circuit layer then can be further bonded to a second circuit layer to provide the vertically interconnected circuit device.

2 Representative Drawing

Figure 1